Lógica Secuencial en VHDL (III)
Timing

• Flip-flop samples D at clock edge
• D must be stable when sampled
• Similar to a photograph, D must be stable around clock edge
• If not, metastability can occur
Input Timing Constraints

• **Setup time:** $t_{\text{setup}} =$ time *before* clock edge data must be stable (i.e. not changing)

• **Hold time:** $t_{\text{hold}} =$ time *after* clock edge data must be stable

• **Aperture time:** $t_a =$ time *around* clock edge data must be stable ($t_a = t_{\text{setup}} + t_{\text{hold}}$)
Output Timing Constraints

- **Propagation delay:** $t_{pcq} = \text{time after clock edge that the output } Q \text{ is guaranteed to be stable (i.e., to stop changing)}$
- **Contamination delay:** $t_{ccq} = \text{time after clock edge that } Q \text{ might be unstable (i.e., start changing)}$
Dynamic Discipline

• Synchronous sequential circuit inputs must be stable during aperture (setup and hold) time around clock edge

• Specifically, inputs must be stable
  – at least $t_{\text{setup}}$ before the clock edge
  – at least until $t_{\text{hold}}$ after the clock edge
Dynamic Discipline

- The delay between registers has a **minimum** and **maximum** delay, dependent on the delays of the circuit elements.
Setup Time Constraint

- Depends on the **maximum** delay from register R1 through combinational logic to R2
- The input to register R2 must be stable at least $t_{\text{setup}}$ before clock edge

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}})$$
Hold Time Constraint

- Depends on the **minimum** delay from register R1 through the combinational logic to R2
- The input to register R2 must be stable for at least $t_{\text{hold}}$ after the clock edge

\[ t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}} \]
\[ t_{\text{cd}} > t_{\text{hold}} - t_{\text{ccq}} \]
Timing Analysis

**Timing Characteristics**

- \( t_{ccq} = 30 \text{ ps} \)
- \( t_{pcq} = 50 \text{ ps} \)
- \( t_{setup} = 60 \text{ ps} \)
- \( t_{hold} = 70 \text{ ps} \)
- \( t_{pd} = 35 \text{ ps} \)
- \( t_{cd} = 25 \text{ ps} \)

\[ t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps} \]

\[ t_{cd} = 25 \text{ ps} \]

**Setup time constraint:**

\[ T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps} \]

\[ f_c = 1/T_c = 4.65 \text{ GHz} \]

**Hold time constraint:**

\[ t_{ccq} + t_{cd} > t_{hold} \]?

\[ (30 + 25) \text{ ps} > 70 \text{ ps} \] ? **No!**
Timing Analysis

Add buffers to the short paths:

Timing Characteristics

\[ t_{ccq} = 30 \text{ ps} \]
\[ t_{pcq} = 50 \text{ ps} \]
\[ t_{setup} = 60 \text{ ps} \]
\[ t_{hold} = 70 \text{ ps} \]
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Setup time constraint:

\[ T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps} \]
\[ f_c = \frac{1}{T_c} = 4.65 \text{ GHz} \]

Hold time constraint:

\[ t_{ccq} + t_{cd} > t_{hold} ? \]
\[ (30 + 50) \text{ ps} > 70 \text{ ps} ? \text{ Yes!} \]
Clock Skew

- The clock doesn’t arrive at all registers at the same time
- **Skew:** difference between two clock edges
- Perform **worst case analysis** to guarantee dynamic discipline is not violated for any register – many registers in a system!
Setup Time Constraint with Skew

- In the worst case, CLK2 is earlier than CLK1

\[ T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew} \]

\[ t_{pd} \leq T_c - (t_{pcq} + t_{setup} + t_{skew}) \]
Hold Time Constraint with Skew

• In the worst case, CLK2 is later than CLK1

\[ t_{ccq} + t_{cd} > t_{hold} + t_{skew} \]

\[ t_{cd} > t_{hold} + t_{skew} - t_{ccq} \]