GROUP OF COMPUTER ARCHITECTURE

MSI and MESI Protocols
- MSI Protocol.
- MESI Protocol.
<table>
<thead>
<tr>
<th>Request</th>
<th>State</th>
<th>Action type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read hit</td>
<td>S o M</td>
<td>Hit</td>
<td>Read data in local cache.</td>
</tr>
<tr>
<td>Read miss</td>
<td>I</td>
<td>Miss</td>
<td>Place read miss on bus.</td>
</tr>
<tr>
<td>Read miss</td>
<td>S</td>
<td>Replacement</td>
<td>Address conflict miss. Place read miss on bus.</td>
</tr>
<tr>
<td>Read miss</td>
<td>M</td>
<td>Replacement</td>
<td>Address conflict miss. Write back block, place read miss on bus</td>
</tr>
<tr>
<td>Write hit</td>
<td>M</td>
<td>Hit</td>
<td>Write data in local cache.</td>
</tr>
<tr>
<td>Write hit</td>
<td>S</td>
<td>Coherence</td>
<td>Place invalidate on bus.</td>
</tr>
<tr>
<td>Write miss</td>
<td>I</td>
<td>Miss</td>
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<tr>
<td>Read miss</td>
<td>S</td>
<td>-</td>
<td>Shared cache or memory service miss</td>
</tr>
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<td>Read miss</td>
<td>M</td>
<td>Coherence</td>
<td>Attempt to share data. Place cache block on bus and transition to shared.</td>
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<tr>
<td>Invalidate</td>
<td>S</td>
<td>Coherence</td>
<td>Attempt to write shared block. Invalidate block.</td>
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<tr>
<td>Write miss</td>
<td>M</td>
<td>Coherence</td>
<td>Attempt to write block that is exclusive elsewhere. Write-back cache block and make state invalid.</td>
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</table>
Protocol

- **States:**
  - Invalid (I): Invalid block.
  - Shared (S): One or several copies of block.
  - Dirty or Modified (M): Only one copy.

- **Processor Events:**
  - PrRd: Processor Read.
  - PrWr: Processor Write.

- **Processor Transactions:**
  - BusRd (read): Request a copy of block without modifying.
  - BusRdX (read exclusive): Request a copy to modify.
  - BusWB (write back): Update memory.

- **Actions:**
  - Update state, perform transaction through bus and dump value to bus.
- Replacements and write backs not shown.
- No bus transactions due to:
  - Rd/Wr in M state.
  - Rd in S state.
- Two bus transactions for:
  - Rd/Wr in I state.
- Wr in S state causes two bus transactions:
  - Block transition to modified.
  - Transition can be avoided as data is already there:
    - BusUpgr instead of BusRdx
Read and modify data are two bus transactions even if not shared.

- Even in sequential programs!
- BusRd (I->S) followed by BusRdX or BusUpgr (S->M)

Solution:
- Add new state: Exclusive (E).

States:
- M: Modified (dirty).
- E: Exclusive (single non-modified copy).
- S: Shared.
- I: Invalid
- MSI Protocol.
- MESI Protocol.
- **Hit**: No transaction in bus in E state.

- **Transitions from I**:
  - To E with PrRd if no other processor has copy.
  - To S, otherwise.

- **S**, additional signal on bus.

- **BusRd(S)**: If processor keeps block, set S signal to 1.