Analog Integrated Circuit Design

Exercise 1

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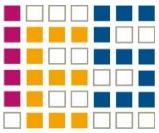

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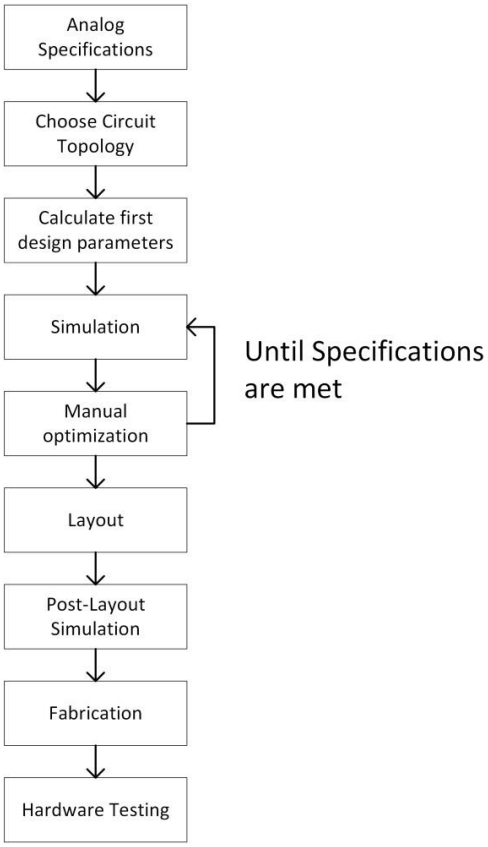
Pre-Assignments

The lecture "*Analog Integrated Circuit Design*" aims at teaching the basic principles, basic circuit blocks and the basic working methods that an analog designer needs to know.

Nowadays, microchips have a high amount of digital components on them. Nevertheless, analog signal processing is still very important before an analog-to-digital converter converts the signal for further digital signal processing. Therefore, we will learn a lot about analog signal processing.
The following figure shows an example of an analog design flow.



To meet the given specifications it is important to know about the different building blocks and to know the different methods to calculate the parameters of such a circuit. Therefore, this exercise aims at practicing the different methods by applying them to several schematics.

Please prepare the following exercises before the exercise session. The results will be needed during the lesson.

In this exercise you will

- deepen your knowledge about the basic principles of BJTs and MOSFETs
- practice a method to calculate Q-points while using the Kirchhoff's voltage and current laws
- get more familiar with the small signal equivalent circuit of BJTs and MOSFETs

Exercise 1.1: Transistor Basics

Recap the basic principles of the bipolar as well as the MOS transistors. Therefore, please fill in the following table:

Characteristic	**BJT**	**MOSFET (enhancement mode)**
Different Types and their symbols		
Current equations in the different operating conditions and their prerequisites	Cutoff Forward-active region	Off Linear region Saturation region
Transconductance g_m (equation)	Forward-active region	Saturation Region
Output resistance r_o (equation)	Forward-active region	Saturation Region
Small Signal Model	NPN	NMOS

Which effect has to be taken into account if the small signal output resistance cannot be neglected? How does this effect influence the output transfer characteristic?		

Exercise 1.2: Methodology

a) Write down the different steps for the Q-point analysis (DC-Analysis).

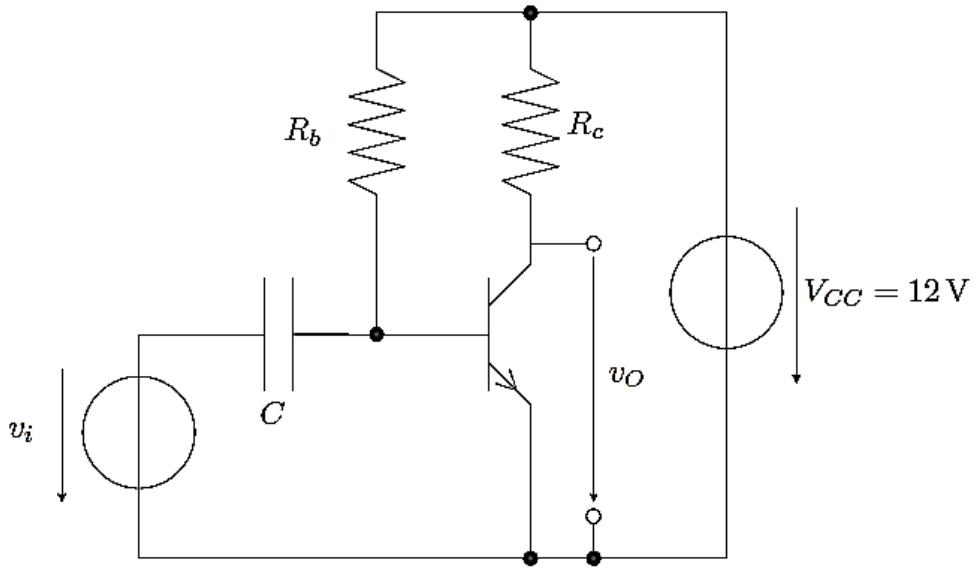
b) Please explain in your own words, what the Kirchoff's Voltage Law and the Kirchhoff's Current Law say.

c) Write down the different steps for the AC-analysis.

Presence Exercises

Exercise 1.3: Q-point and small signal equivalent circuit

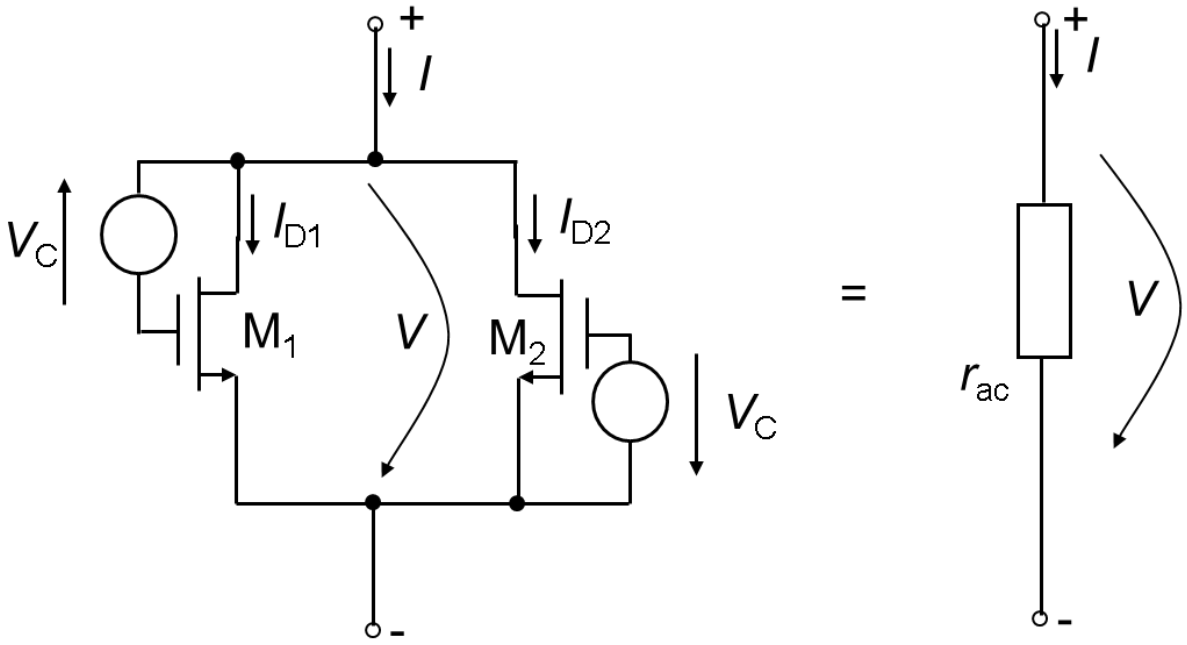
a) Find the value of the resistor R_b if $V_{OQ}=2V$ (whereby V_{OQ} is the output voltage in the Q-point) for $R_c=500\Omega$.
b) Draw the small signal equivalent circuit and replace the transistor with its small signal model.
c) Compute the small signal voltage amplification $A_v=v_o/v_i$.
You may assume $\beta_F=100$ and $V_{BE}=0.7V$.



Exercise 1.4: MOS-Resistors

Given is the following circuit (next page), which acts as an active resistor, with two identical NMOS transistors. You may assume the following parameters: W/L=4, $K'_N=24\mu A/V^2$, $V_{T0}=0.75V$. Note that $K_N=K'_N*W/L$.

a) What should be the value of V_C if an ac equivalent resistance $r_{ac}=2k\Omega$ is required? For which values of the voltage V is the circuit expected to operate in the linear mode?
b) Let the transistor M_1 be removed. Determine the voltage V_C which corresponds to an ac resistance of 2kΩ for the case $V_{DS}=3V$.



Note that Bulk is connected to V_{SS} for both transistors

Analog Integrated Circuit Design

Exercise 2

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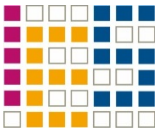

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Pre-Assignments

Please prepare the following exercises before the exercise session. The results will be needed during the lesson.

In this exercise you will

- deepen your knowledge about different current mirror configurations
- practice to draw the small signal equivalent circuit for complex schematics
- practice to calculate the voltages, currents and gains of different circuits
- gain basic knowledge about reference / bias circuits

Exercise 2.1: Current Mirror Basics

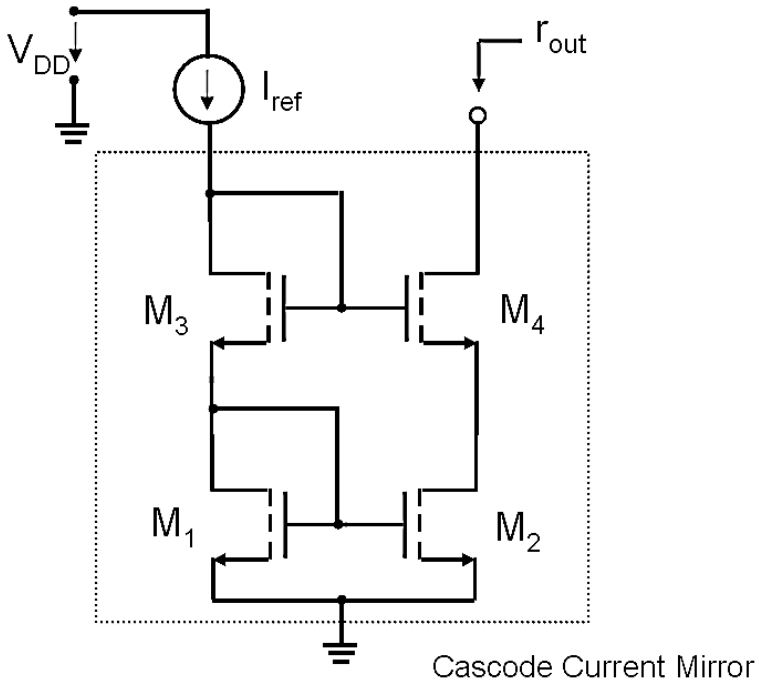
Recap the basic principles of current mirrors from the script.

a) Draw a simple current mirror and explain the working principle in your own words.

b) In which operating condition are the transistors of current mirrors working? Why?

Exercise 2.2: Cascode Current Mirror

The schematic of a cascode current mirror is shown below. You may assume that the transistors M_1=M_2 and M_3=M_4 are properly matched. I_{ref} is a constant current, V_{DD} a constant supply voltage. I_{ref} and V_{DD} are chosen in a way that the circuit is operating properly. For all transistors you may assume $g_m >> g_{ds}$ (with $g_{ds}=1/r_o$).



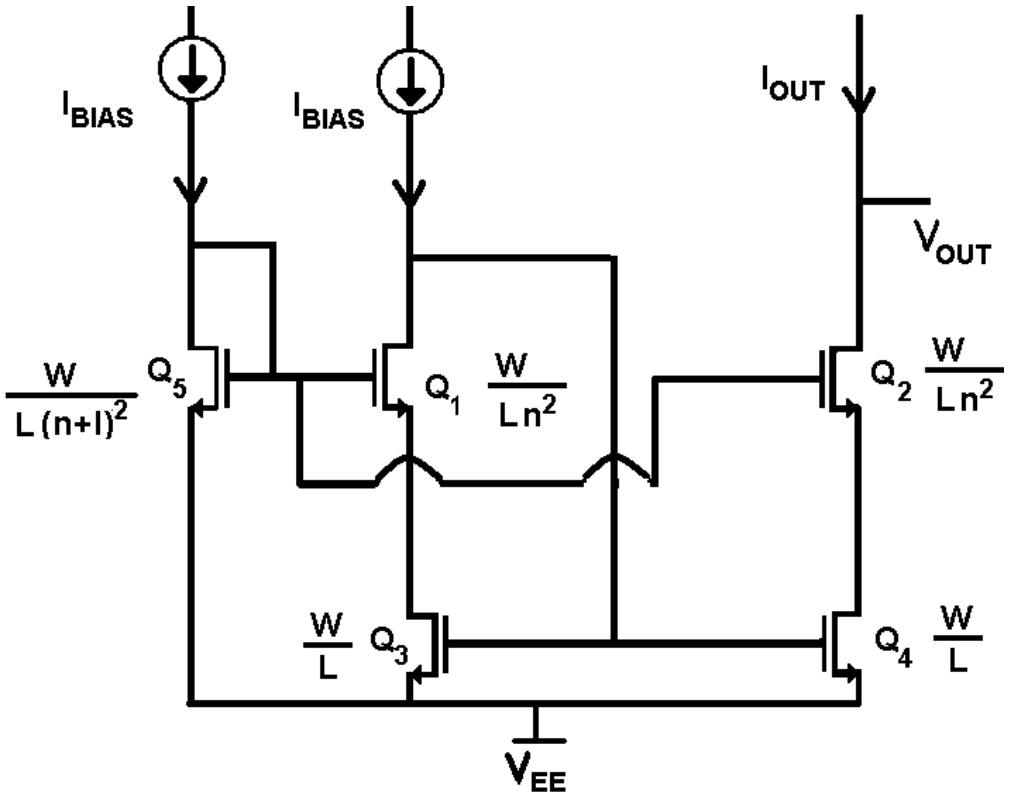
a) Draw the small signal equivalent circuit.

b) Calculate the small signal output resistance r_{out}.

Presence Exercises

Exercise 2.3: WideswingCascode Current Mirror

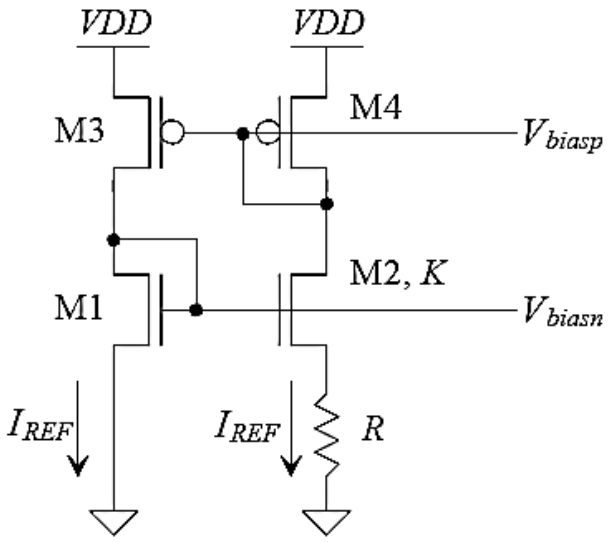
Given below is a wideswingcascode current mirror. Answer the questions given on the next slide. Assume all transistors have the same threshold voltages V_T, $K_N' = \mu_N \cdot C_{ox}$ and channel length modulation effects can be neglected.



a) What is the minimum output voltage V_{out} required so that the transistors Q_2 and Q_4 remain in saturation? Express the answer in relation to the bias voltage ($V_{DS2,sat}=V_{GS2}-V_T$) of transistor Q_2.
b) Prove through equations that the transistor Q_3 is just in the saturation region.
c) Check additionally for which bias voltage V_{GS1} the transistor Q_1 will be in saturation.

Exercise 2.4: Self Biased Current Reference

Given below is a self biased current reference, meaning that the current reference is independent of the supply voltage. Assume the transistors M3,M4 have same W/L ratio of 1:1 and the transistors M1,M2 have a ratio of 1:K. Assume a threshold voltage of V_{TP}&V_{TN} , K_N‘=$\mu_N \cdot C_{ox}$ andK_P‘=$\mu_P \cdot C_{ox}$ as well that channel length modulation is neglected.



Show that the current reference given below is independent of the power supply voltage V_{DD}.

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Exercise 3

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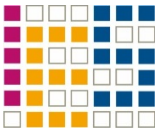

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Pre-Assignments

Please prepare the following exercises before the exercise session. The results will be needed during the lesson.

In this exercise you will

- deepen your knowledge of voltage and current references
- use your expertise of small signal equivalent circuits and circuit analysis to calculate the specifications of a circuit (such as gain, r_{in}, r_{out},…).
- refresh your knowledge of single stage amplifiers and their configurations.

Exercise 3.1: Supply Voltage Independent and Bandgap Reference

Recap the basic principles of bandgap references from the script.

a) How can you calculate the sensitivity of an output voltage with respect to the supply voltage? Explain your approach if you were given a schematic.

b) Explain in your own words the principle of bandgap references.

Exercise 3.2: Multistage Amplifiers

a) Recap the different configurations of single stage amplifiers (common-…). How do they look like? How can you identify them in a multistage amplifier? What are their main purposes/advantages?

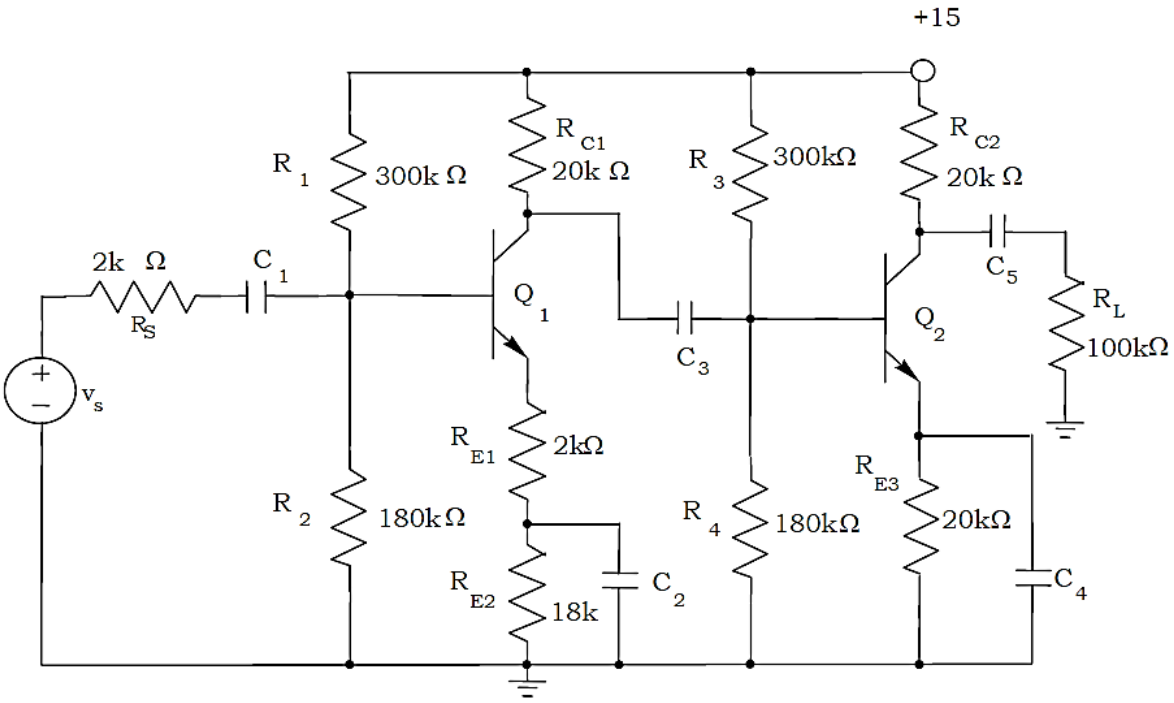
b) Recap the different steps to perform a DC analysis to calculate the Q-point of a circuit.

c) How do you calculate the overall gain of a three stage amplifier with A_1, A_2 and A_3 being the amplifications of the three stages.

d) What are the definitions for the small signal input and output resistance r_{in} and r_{out}, respectively?

e) Recap how to draw the small signal equivalent circuit of a circuit.

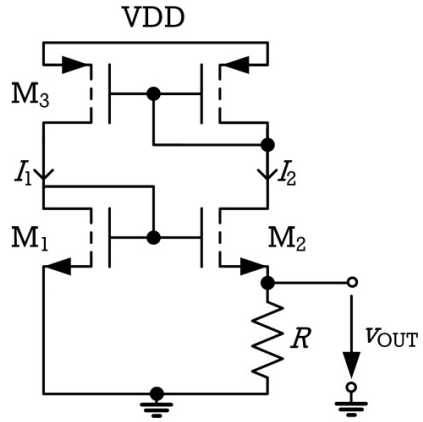
f) Draw the small signal equivalent circuit of the following circuit.



Presence Exercises

Exercise 3.3: Voltage Reference

Given below is the schematic of a voltage reference circuit. Assume that the PMOStransistors (M3,M4) are matched properly. You may further assume that thetransistors M1 and M2 are sized according to the ratio 1:k. You may neglectchannel length modulation effects.

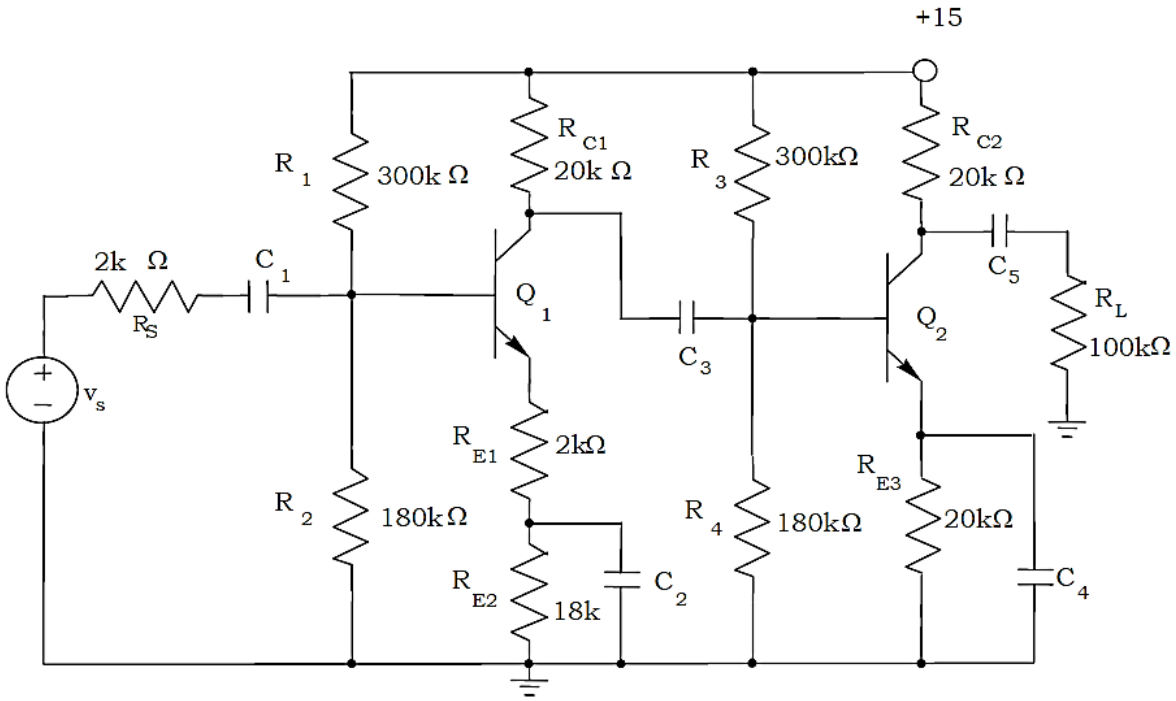


a) Derive the voltage V_{OUT} of the circuit across the resistance R in terms of the circuit parameters. Is the output voltage dependent on the supply voltage? Is it dependent on temperature?

b) Can you think of a circuit that makes a better voltage reference than the one shown above? Draw its schematic.

Exercise 3.4: Two Stage Amplifier

The schematic of a two stage amplifier is given. Use β_F=100 and V_A=70V for all transistors
Use the small signal equivalent circuit from exercise 3.2.



a) Calculatethe Q-points ofthetransistors.
b) Calculatethemidbandvoltagegainofeachstage.
c) Calculatetheoverallmidbandvoltagegain.
d) Calculatetheinputandoutputresistance oft he circuit.

Analog Integrated Circuit Design

Exercise 4

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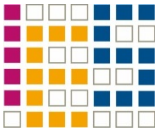

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Pre-Assignments

Please prepare the following exercises before the exercise session. The results will be needed during the lesson.

In this exercise you will

- get a deeper understanding of multistage amplifiers and the differences to differential amplifiers
- analyze a differential amplifier to get a good understanding of its functioning

Exercise 4.1: Single Stage Amplifiers

Recap the basic principles of differential amplifiers.

a)! What are the advantages of differential amplifiers compared to multistage amplifiers?

b)! Which general circuit building blocks can you find in a two-stage opamp?

c)! Which of the following statements is correct? If necessary, correct the answers.

i.! CMRR is the ratio of A_{CM} to A_{DM}

ii.! For a differential amplifier with ideal matched devices CMRR$\rightarrow\infty$

iii.! The half circuit method can also be used for analyzing the input stage of operational amplifiers.

iv.! The half circuit method that we use for calculating the Q-point can also be used for the calculation of the differential mode gain.

d)! What is the difference between Class-A, Class-B, and Class-AB output stages?

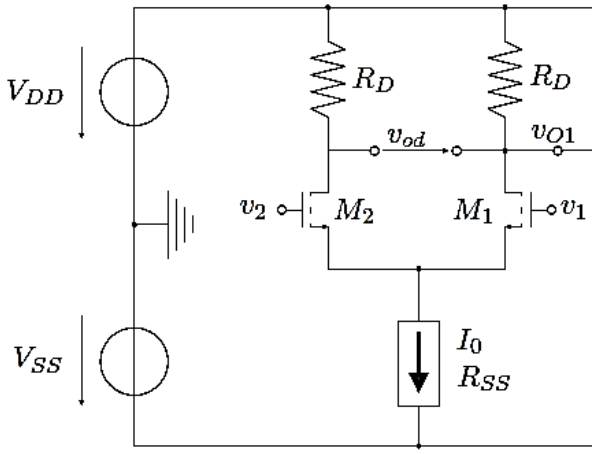
e)! What is the purpose of the additional transistors that can often be found in output stages?

Exercise 4.2: Methodology

Write down the different steps for half circuit analysis.

Exercise 4.3: Differential Amplifier

The schematic of a differential amplifier with resistor load is given. You may assume the following parameters: V_{DD}=12V, V_{SS}=12V, I_0=40µA R_D=300kΩ, R_G=1kΩ, R_L=1kΩ, R_{SS}=500kΩ, K_N=K_P=K=640µA/V^2, V_{TN}=-V_{TP}=V_T=1V, λ_N= λ_P= 0
Analyze the circuit according to the questions a)-c).
Hint: Use the method of half circuit analysis.



a)! Calculate the Q-points of the transistors M_1 and M_2.
Hints:
- ○! Use the steps for DC analysis from preparation of Exercise 1.
- ○! Calculate V_{ds} and V_{gs}.

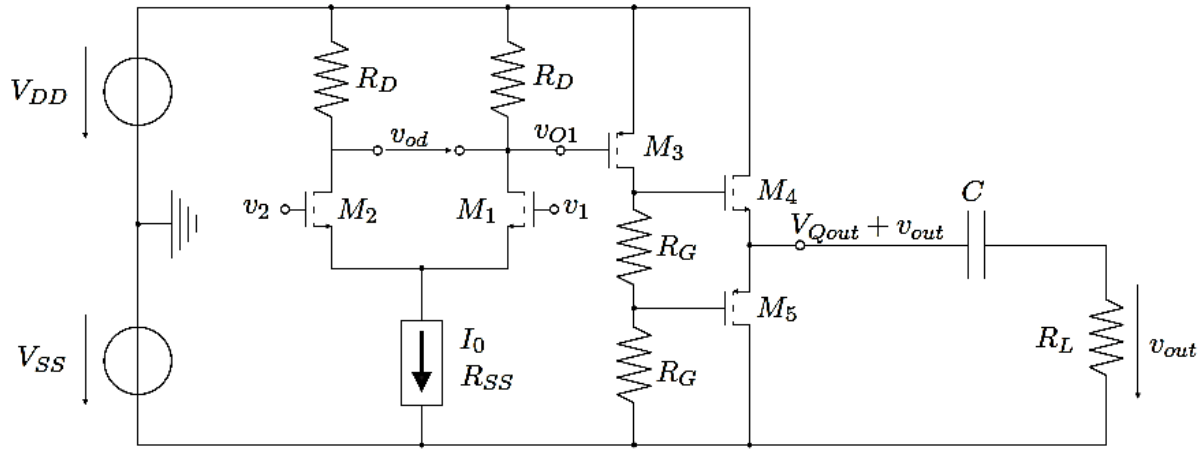
b)! Calculate the differential mode gain A_{DM}, the common mode gain A_{CM} and the CMRR when using v_{o1} as output.
Hints:
- ○! What does the symbol of current source mean for AC / DC?
- ○! A_{DM}: AC Analysis → what happens to node at source of transistor?
- ○! Results: A_{DM}=-24 =27.6dB; A_{CM}=-0.3 =-10.5dB; CMRR=80=38.1dB

c)! Now v_{od} is used for output. How does the result from b) changes?

Presence Exercises

Exercise 4.4: Differential Amplifier

Now the differential stage of Exercise 4.3 is extended by an output stage. Use the parameters as given in Exercise 4.3.



Answer the following questions:

a)! Calculate the Q-point of transistor M_3.
b)! Calculate V_{Qout}.
Hint:
- ○! During DC-Analysis you might find a quadratic equation. Solve it and check the meaningfulness of the two solutions by comparing them to the physical relationships given in the schematic.

c)! Calculate the Q-points of the transistors M_4 and M_5.
Hint:
- ○! Which mode of operation are the transistors in? Linear region or saturation region?

d)! Calculate the differential mode gain A_{DM}, the common mode gain A_{CM} of the complete circuit.
e)! How does the CMRR change compared to 4.3 (b)?
Interpret your results. Which part of the circuit is responsible for the common mode rejection?

Analog Integrated Circuit Design

Exercise 5

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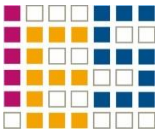


Status: 12.10.2015

Pre-Assignments

Please prepare the following exercises before the exercise session. The results will be needed during the lesson.

In this exercise you will

- apply the SCTC and the OCTC method to different circuits
- refresh some of the methods that you have already learned in previous exercises (small signal equivalent circuit, equivalent resistance,…)

Exercise 5.1: Useful Methods

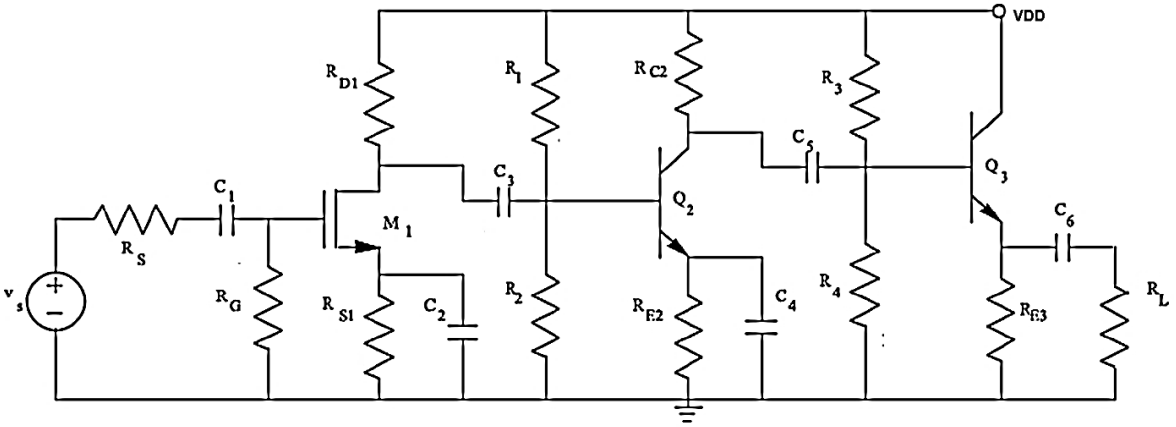
a) Which method is used to estimate the lower cutoff frequency of an amplifier? Write down the different steps that have to be performed.

b) Write down the different steps that have to be performed for the Open-Circuit Time-Constant method. Why does the hybrid-pi model has to be used for calculating the upper cutoff frequency?

c) How do you calculate the equivalent resistance of a circuit?

Exercise 5.2: Multistage Amplifier

The schematic of a multistage amplifier is given in the following.



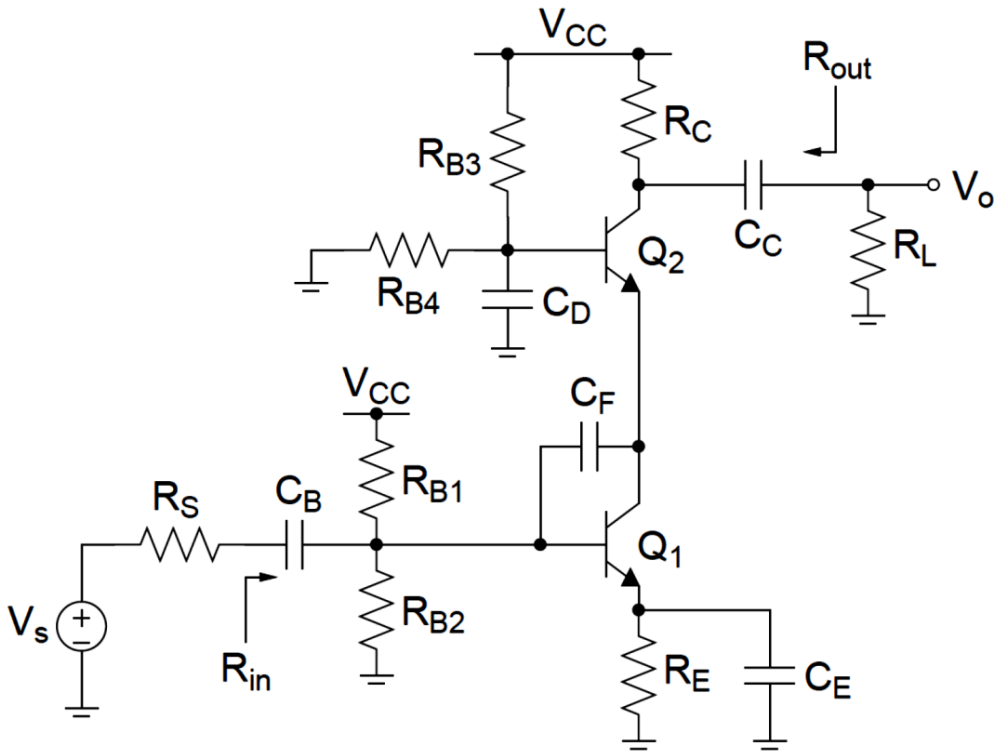
Calculate the lower-cutoff frequency f_L of the amplifier following the steps that you have figured out in Exercise 5.1.
Hints:

- Use the SCTC (Short-Circuit Time Constant) method. The circuit has 6 independent coupling and bypass capacitors.
- For considering the influence of C_2, the output resistance r_o of M_1 can be neglected.
- The output resistance r_o of Q_2 and Q_3 can be neglected when calculating C_4, C_5, C_6.

Presence Exercises

Exercise 5.3: Cascode Amplifier

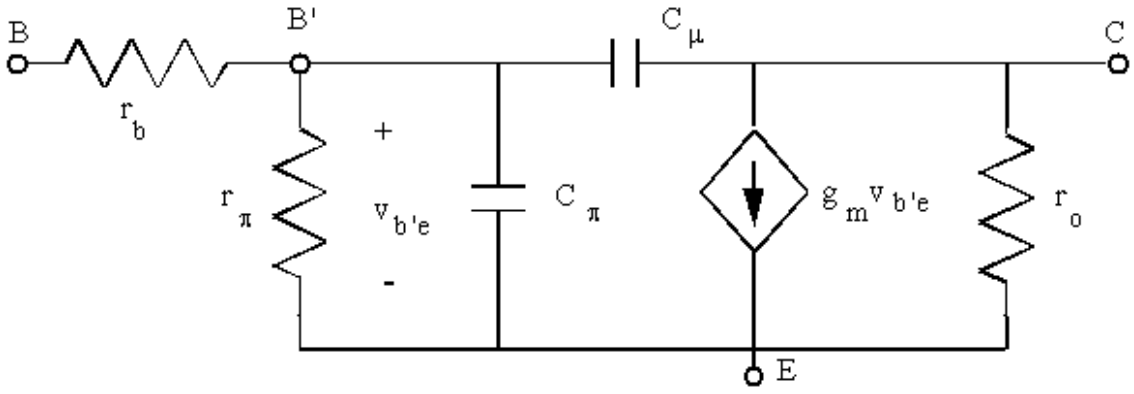
The schematic of a cascode amplifier is given in the following.



Calculate the upper-cutoff frequency f_H of the amplifier following the steps that you have figured out in Exercise 5.1.

Hints:

- Use the OCTC (Open-Circuit Time-Constant) method. Assume that the early effect can be neglected. Use the hybrid pi transistor model.
- Capacitors C_B and C_C are used for AC coupling, whereas C_D and C_E are AC bypass capacitors. C_F is a small capacitance that will be used to control the higher 3-dB frequency of the amplifier.
- Only when calculating the time constant for the capacitance C_μ in the transistor Q_1, assume that the capacitance C_F is connected across B' and C to simplify calculations.



Analog Integrated Circuit Design

Exercise 7

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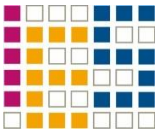

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Pre-Assignments

Please prepare the following exercises before the exercise session. The results will be needed during the lesson.

In this exercise you will

- draw the two-port model of different amplifiers and identify the feedback topology
- deepen your knowledge of the characteristics of the different feedback topologies
- calculate the A and the β-circuit of different amplifiers
- deepen your understanding of the differences between open-loop parameters and closed-loop parameters for the different types of feedback
-

Exercise 7.1: Feedback Topologies

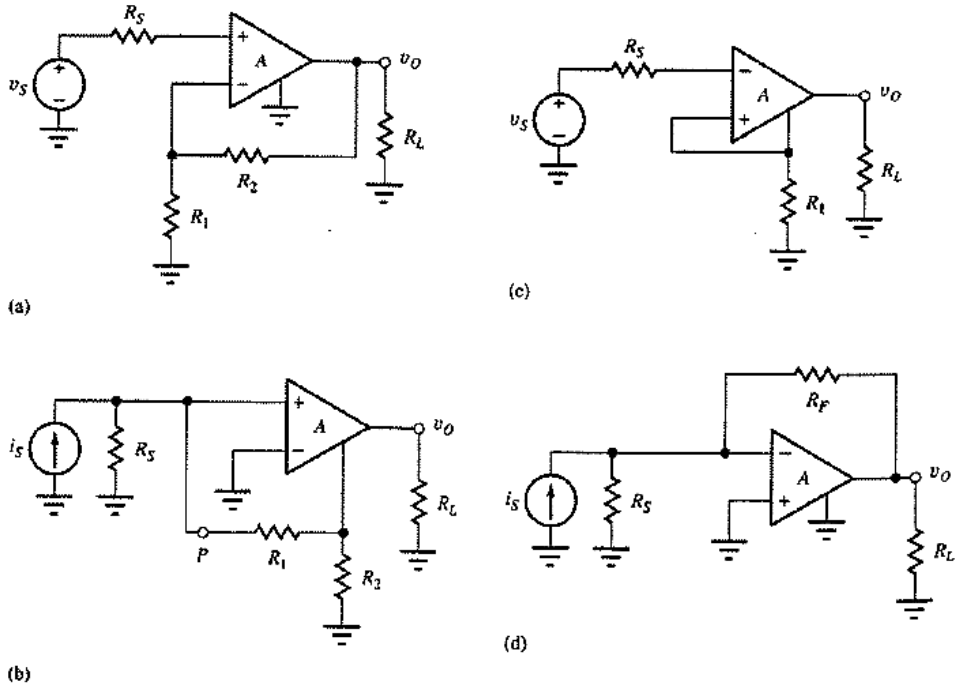
a) Name the four feedback topologies. When do you use which topology?

b) A negative feedback is intended to allow a modification of some characteristics of a particular amplifier. Which feedback topology should be used in the following cases?

i. Input resistance is to be lowered and output resistance to be increased
ii. Both input and output resistance should be increased
iii. Both input and output resistance should be decreased

c) How do you identify the feedback topology in a circuit? Write down your method.

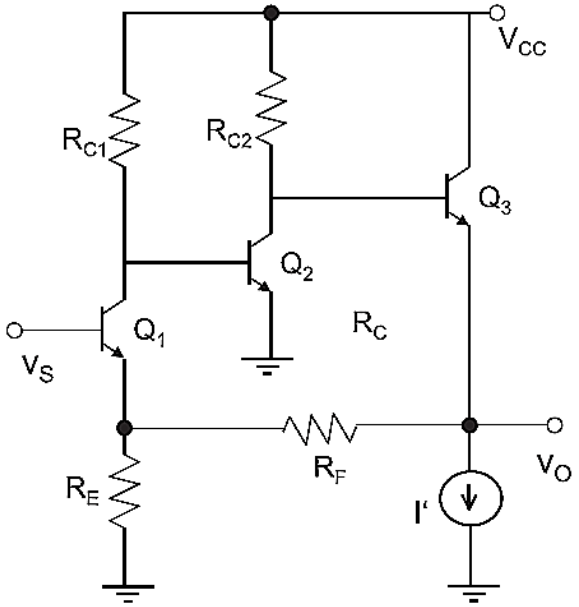
d) Draw the two port model of the circuit and mark the open-loop amplifier (A) as well as the feedback network (F) for the following amplifiers.
Identify their feedback topology.



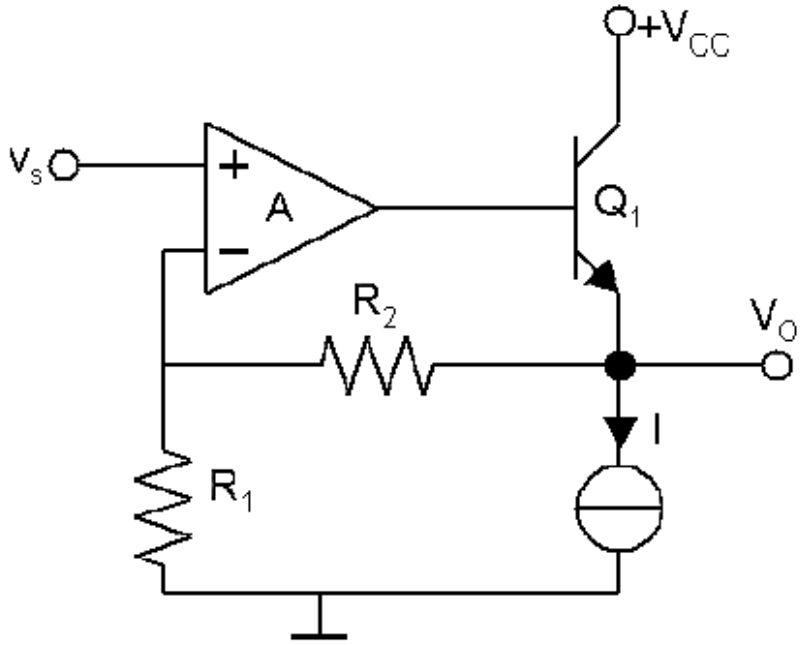
Exercise 7.2: Feedback Topologies

Please identify the feedback topology of the following circuits.

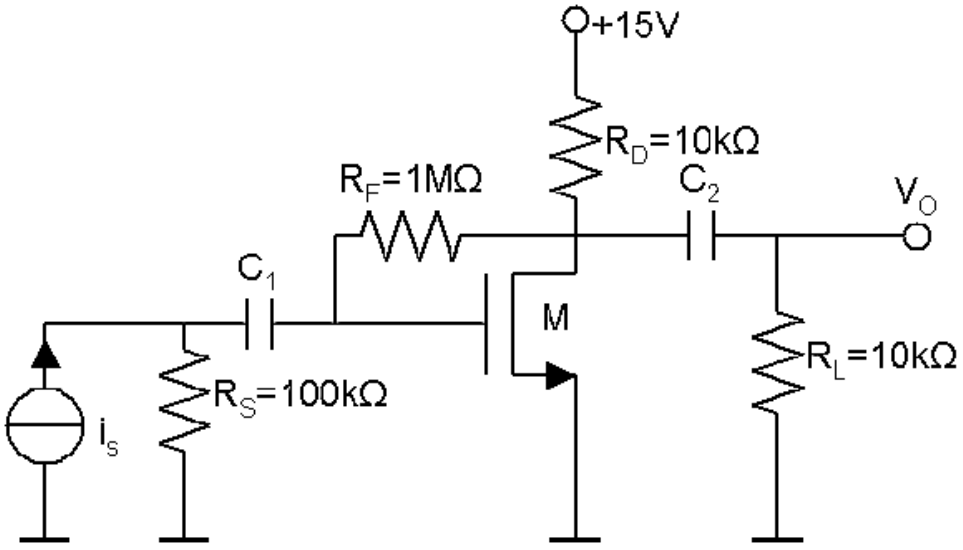
a) Feedback Amplifier I



b) Feedback Amplifier II



c) Feedback Amplifier III



Exercise 7.3: Stability

Which of the following statements about stability are true? If needed, correct the false statements.

i. The stability of a feedback amplifier, depicting a zero phase margin, can be improved by increasing the open loop gain.
ii. If the open loop gain A of a feedback amplifier decreases by 10%, the closed loop gain will increase by 10% at least.

Presence Exercises

Exercise 7.4: Feedback Amplifier I

For the circuit "Feedback Amplifier I" shown in Exercise 7.2 a), answer the following questions.

a) Show that if the open loop gain A is large, then the closed loop voltage gain A_V is given approximately by

$$A_V = \frac{v_o}{v_s} \approx \frac{R_F + R_E}{R_E}.$$

b) If R_E is chosen equal to 50Ω, find the value of R_F that will result in a closed loop gain of approximately 25.
c) If Q_1 is biased at I_{C1}=1mA, Q_2 at I_{C2}=2mA and Q_3 with I_{C3}=5mA, and assuming that all transistors have β=100, find approx. the values for R_{C1} and R_{C2} to obtain gains from the stages of the feedforward circuit as follows: a voltage gain of about -10 for Q_1 and a voltage gain of about -50 for Q_2.
d) For your design, what is the closed loop voltage gain realized?
e) Calculate the input and output resistances of the closed-loop amplifier designed.

Exercise 7.5: Feedback Amplifier II

For the circuit "Feedback Amplifier II" shown in Exercise 7.2 b), the following parameters are known: R_1=1kΩ, R_2=7.5kΩ, β_0=100, R_{iD}=40kΩ (input resistance of the opamp for the differential mode), I_0=200µA, V_{CC}=10V, A=50dB, R_{out}=0Ω. The input resistance for the common mode is neglected / assumed to be infinite.

Calculate the following circuit characteristics:

a) The voltage gain A_v
b) The input resistance R_{in}
c) The output resistance R_{out}

Exercise 7.6: Feedback Amplifier III

For the circuit "Feedback Amplifier III" shown in Exercise 7.2 c), the following parameters are known: g_m=2mS, r_0=40kΩ

Calculate the following circuit characteristics:

a) The midband transresistance A_{TR}
b) The input resistance R_{in}
c) The output resistance R_{out}

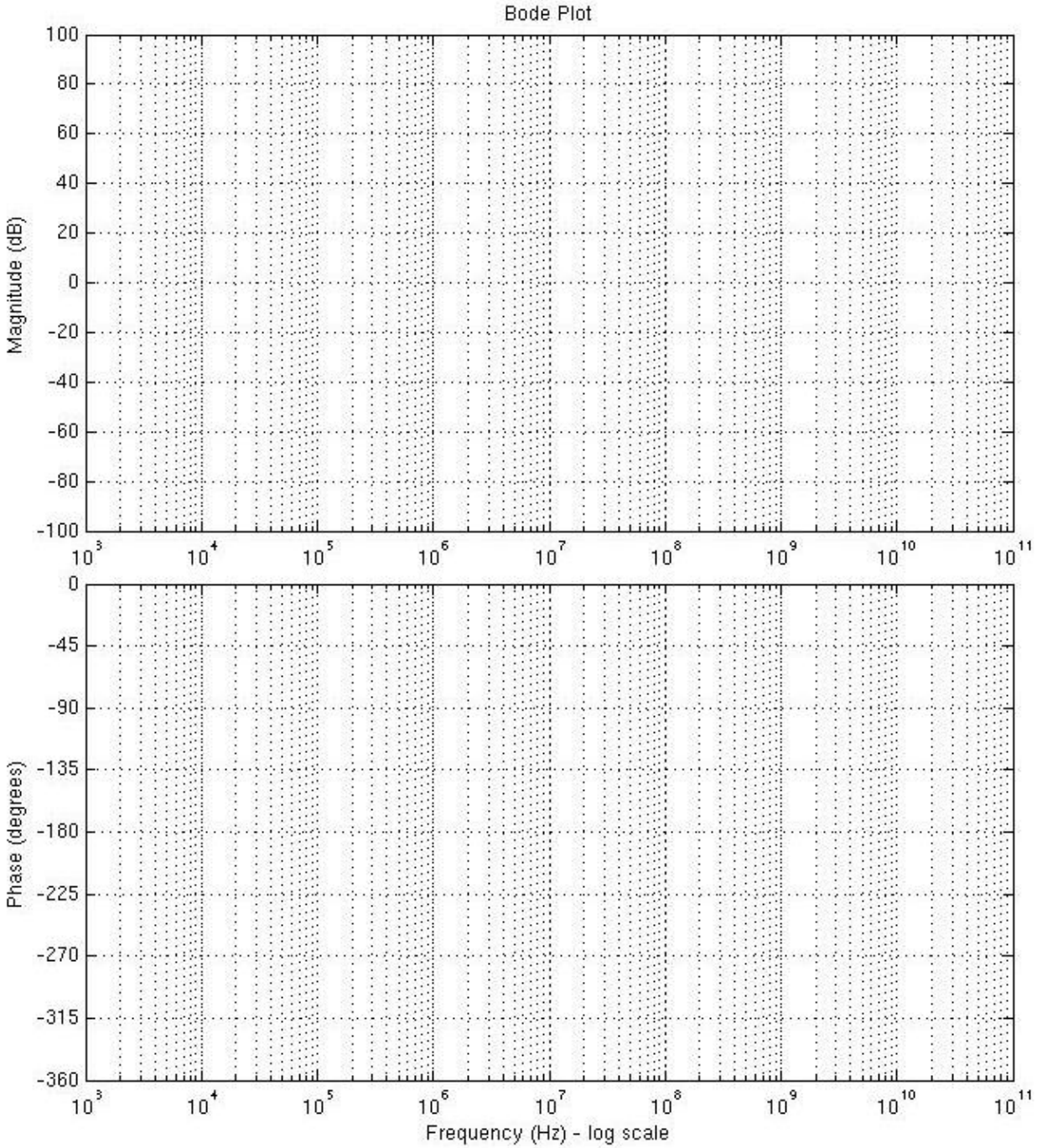
Exercise 7.7: Transfer Functions

The closed-loop transfer function of a system is given by

$$A(s) = \frac{10^6 s + 10^{15}}{s^2 + 1.01 \cdot 10^7 s + 10^{12}}$$

Use the transfer function to answer the following questions.

a) How many poles and zeros does the system have?
b) Calculate the location of the poles and zeros. At which frequencies are these located? Express your answer in Hz.
c) Calculate the low-frequency (i.e., DC) gain of this system? Express your answer in decibels.
d) Draw the magnitude and phase response of the system in the graph given on the next page. Mark the poles, zeros, the DC Gain, the unity-gain frequency and the slope of the magnitude response in the plot.
e) Calculate the phase margin of the system from the plots.


Bode Plot
Magnitude (dB)
100
80
60
40
20
0
-20
-40
-60
-80
-100
Phase (degrees)
0
-45
-90
-135
-180
-225
-270
-315
-360
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^{10}
10^{11}
Frequency (Hz) - log scale

Analog Integrated Circuit Design

Exercise 8 and 9

Integrated Electronic Systems Lab
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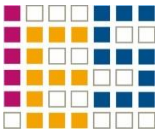


Status: 12.10.2015

Pre-Assignments

Please prepare the following exercises before the exercise session. The results will be needed during the lesson.

In this exercise you will

- deepen your knowledge of switched capacitor circuits
- derive the transfer function of a switched capacitor circuit
- deepen your knowledge of ADCs and DACs as well as their characteristics

Exercise 8.1: Switched Capacitors

a) Explain the principle of switched capacitors in your own words? How does this method emulate resistors? Derive the equation for the equivalent resistance.

b) Why are switched capacitors preferred to resistors in integrated circuits?

Exercise 9.1: ADCs and DACs

a) Name the ADC architectures introduced in the script and explain their working principle in your own words.

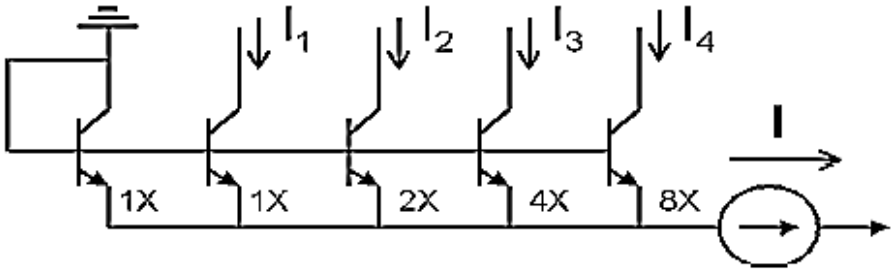
b) Name the DAC architectures introduced in the script and explain their working principle in your own words.

c) Why is the weighted-resistor DAC not suitable for single-chip integration solutions?

d) What kind of AD converter can be used in the following case: bandwidth: 500kHz, resolution: 12bits, sampling rate: 1MHz. Assume: ADC clock frequency = sampling rate. Choose one of the following converter types:
   - Parallel (flash) converter
   - Successive approximation converter
   - Counting converter
   - Single-ramp converter

   Hint: What are the conversion times of the different ADCs?

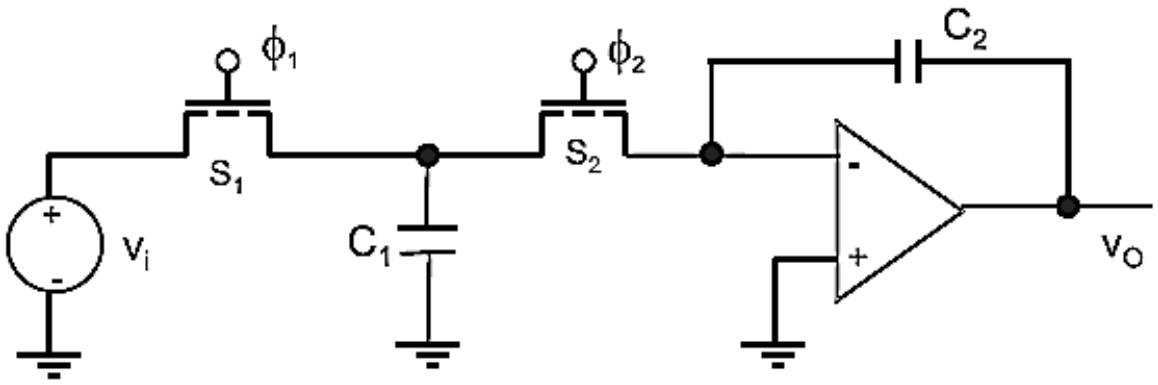
e) The circuit shown below is intended to be used in a DAC based on the switching of binary weighted current sources. Find the currents I_1, I_2, I_3 and I_4.
Hint: Consider the scaling factors of the emitter-base junction areas.



Presence Exercises

Exercise 8.2: Switched Capacitor Circuit

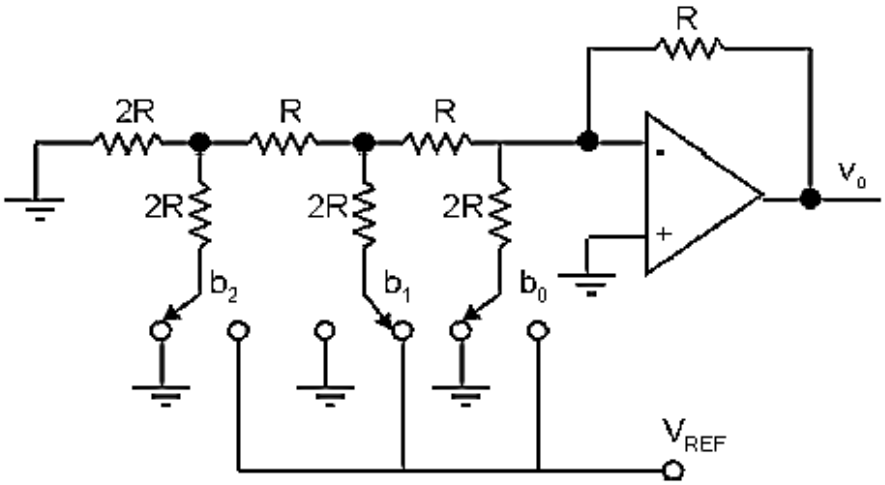
Given below is a switched capacitor circuit. Please answer the following questions.



a) A clock frequency of 100kHz is used in the switched capacitor circuit shown on the next page. What input resistance corresponds to C_1 capacitance values of 1pF and 10pF?
b) For a dc voltage of 1V applied to the input of the circuit shown on the next page, in which C_1 is 1pF, what charge is transferred for each cycle of the two-phase clock?
c) For a 100kHz clock, what is the average current drawn from the input source? For a feedback capacity C_2 of 10pF, what change should be expected in the output for each cycle of the clock?
d) For an amplifier that saturates at ±10V and the feedback capacitor being discharged, how many clock cycles would it take to saturate the amplifier? What is the average slope of the staircase output voltage produced?

Exercise 9.2: R-2R-Ladder

Given below is the schematic of a 3bit R-2R-Ladder. Answer the following questions.

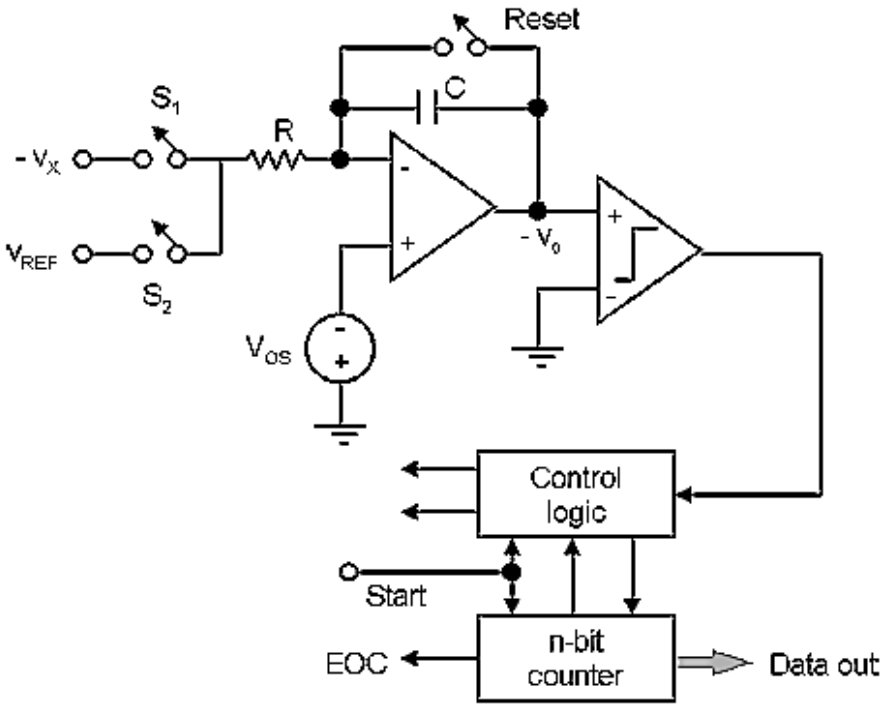


a) Find the output voltage v_o in the given R-2R ladder for the input bit sequence 101 (V_{REF}=2V).
Hint: Redraw the schematic using the Thévenin Equivalent. The amplifier will then look like a simple inverting. What is V_{eq} and R_{eq}?

b) For an offset voltage V_{OS} of -150mV and a feedback resistance value of $1.05 \cdot R$, determine the gain and offset errors for the bit sequences 101 and 010.
Hint: See Script Slide 489-491.

Exercise 9.3: Dual Ramp AD-Converter

The following circuit has been designed to be a dual-ramp AD converter. 128µs are required for the first integration while converting a voltage of 2V. Furthermore the following values are known: f_{clk}=1MHz, V_{REF}=3V.



a) Determine the ADC resolution.
   Hint: How is T_1 usually chosen? Interpret from the equation in the script.
b) How long should it take to perform a complete conversion for an input voltage of 2.5V?
c) A voltage peak value of 4.64V has been reached during the conversion of a voltage of 2V. Find the time constant of the converter.