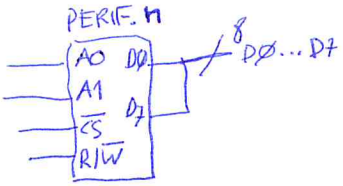
TEMA 5 (EJERCICIOS)

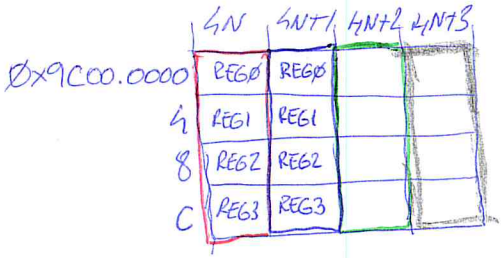
EJERCICIO 1

4 PERIFÉRICOS 8 bits (4 REGISTROS)

0x9C00.0000 → $\overline{EMC\_CS3}$

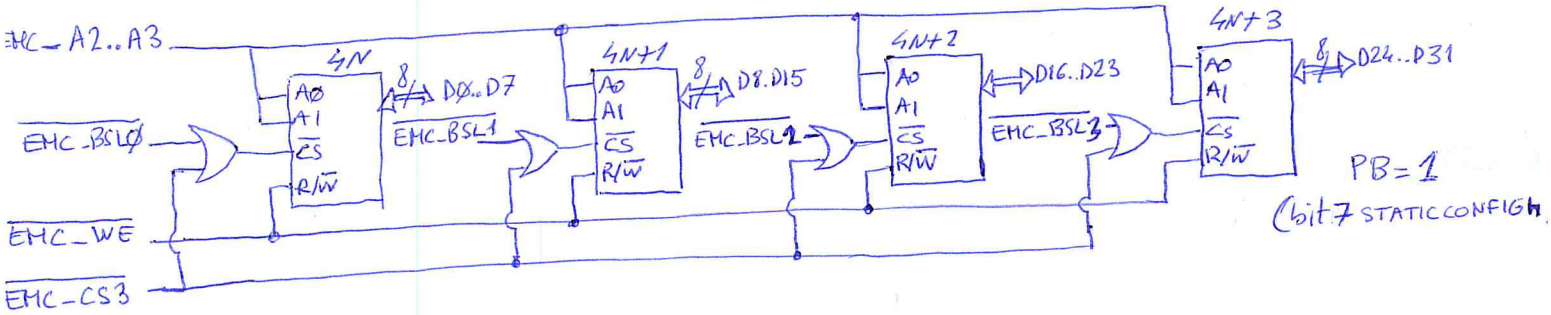
MODO 32 bits (MW = 00) → 4 BANCOS





— PERIF 1
— PERIF 2
— PERIF. 3
— PERIF. 4

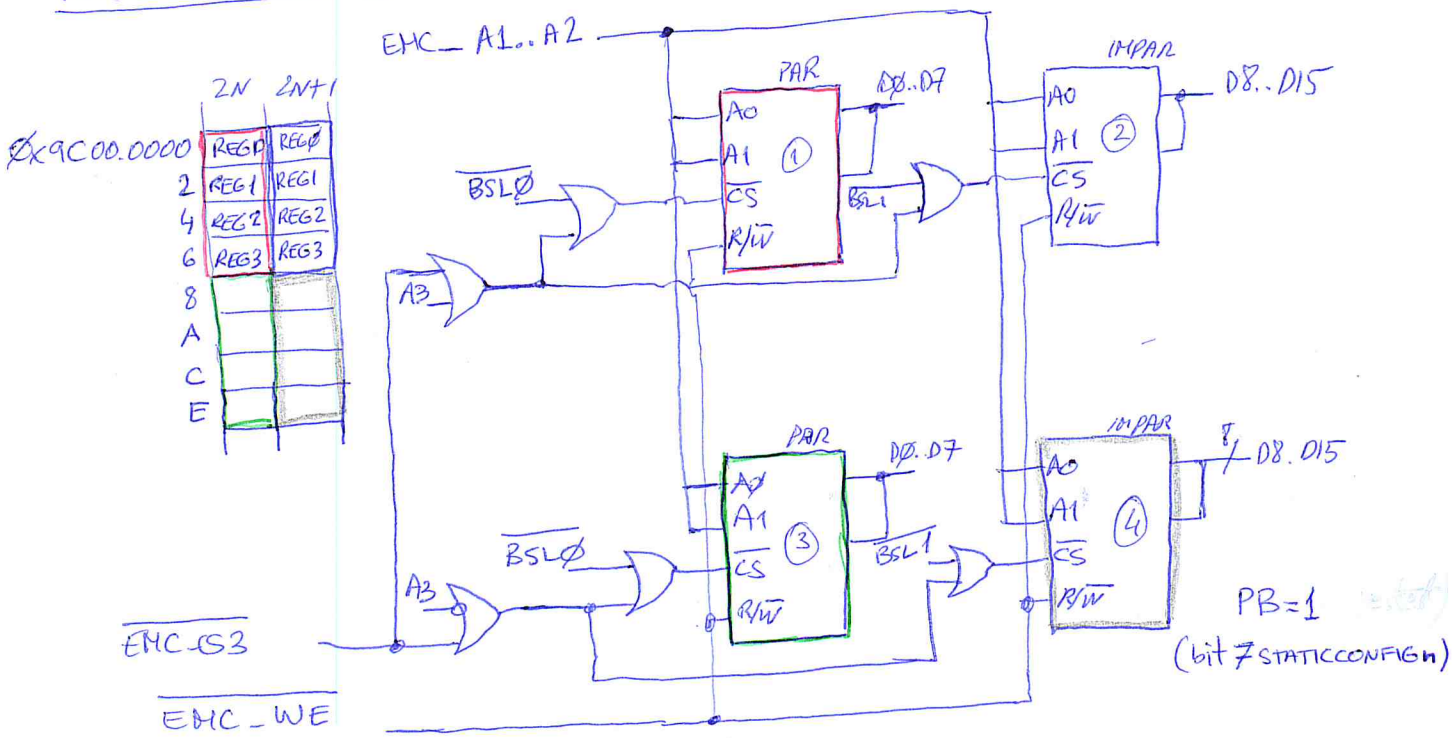
LITTE-ENDIAN (Reset) !



PB = 1
(bit 7 STATICCONFIGn)

MODO 16 bits (MW = 01) 2 BANCOS

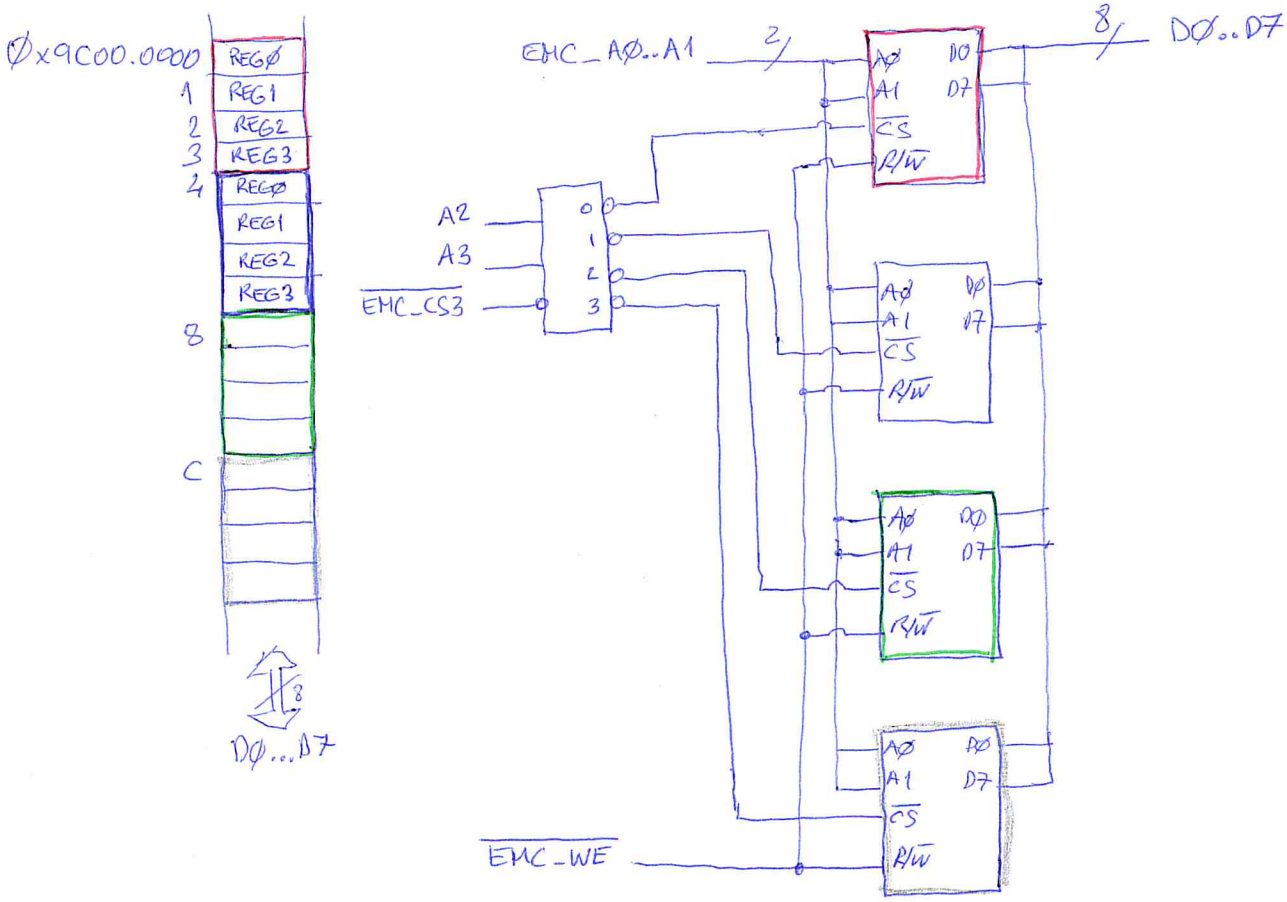
LITTLE-ENDIAN (Reset)



PB = 1
(bit 7 STATICCONFIGn)

EJERCICIO 1 (Continuación)

MODO 8 bits (MW = 00) reset



Ojo! No intervienen las líneas de selección de banco (EMC_BLSn)

EJERCICIO 2

ROM ___ 1 Mbyte (4 x 256K x 8)

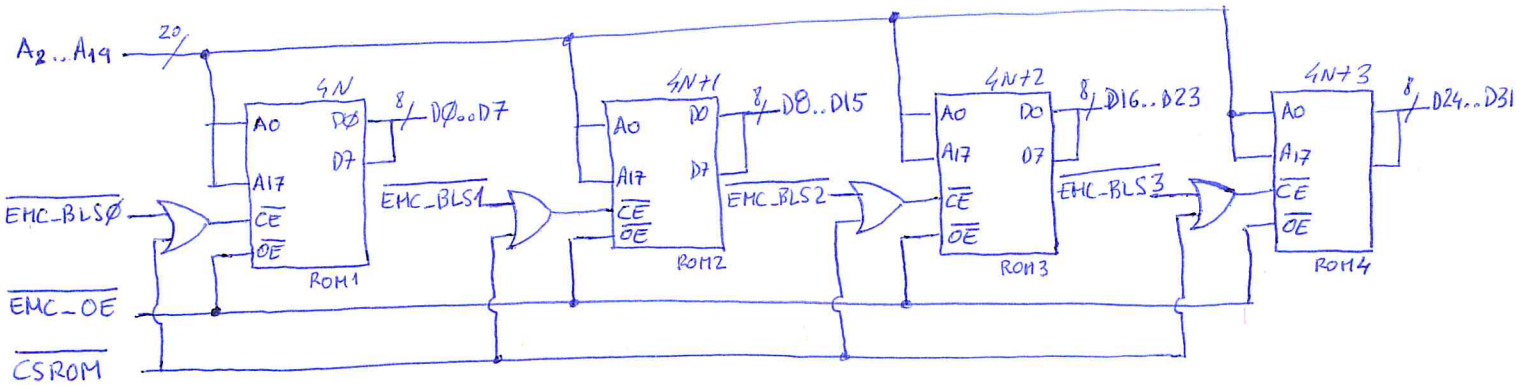
RAM ___ 128 Kbytes (4 x 32K x 8)

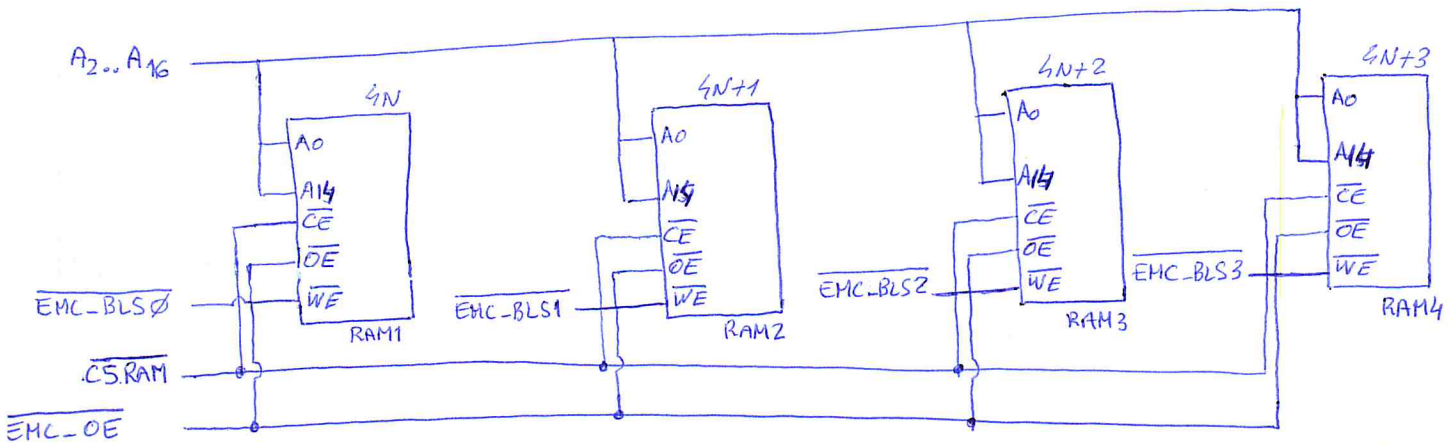
MODO 32 bits (4 bancos)

DIRECCIONES	
Øx8000.0000 ØxBØØF.FFFF	ROM (1 Mbyte)
Øx8Ø1Ø.0000 Øx8Ø11.FFFF	RAM (128 Kbytes)

$\overline{CSROM} = A20 + \overline{EMC\_CSØ}$

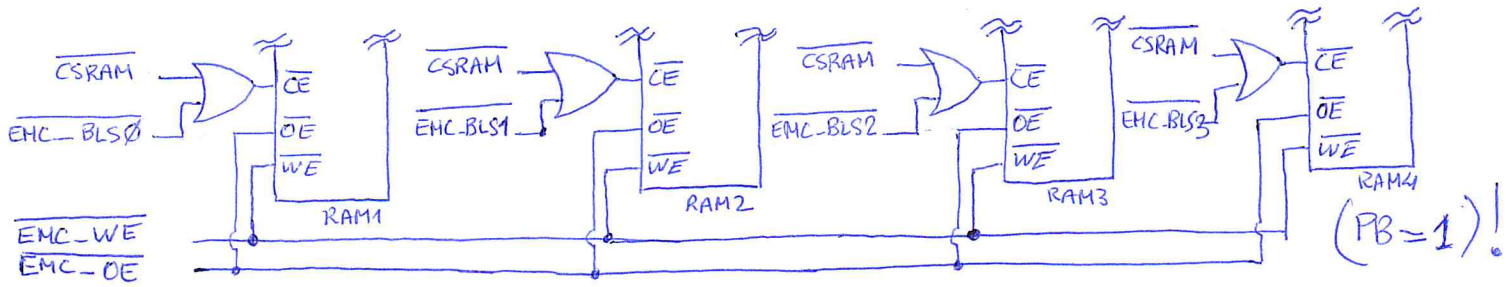
$\overline{CSRAM} = \overline{A20} + A19 + A18 + A17 + \overline{EMC\_CSØ}$





* Sólo se activan BLSn en escritura !!

ojo! ($PB^{*} = 0$)



(PB = 1) !

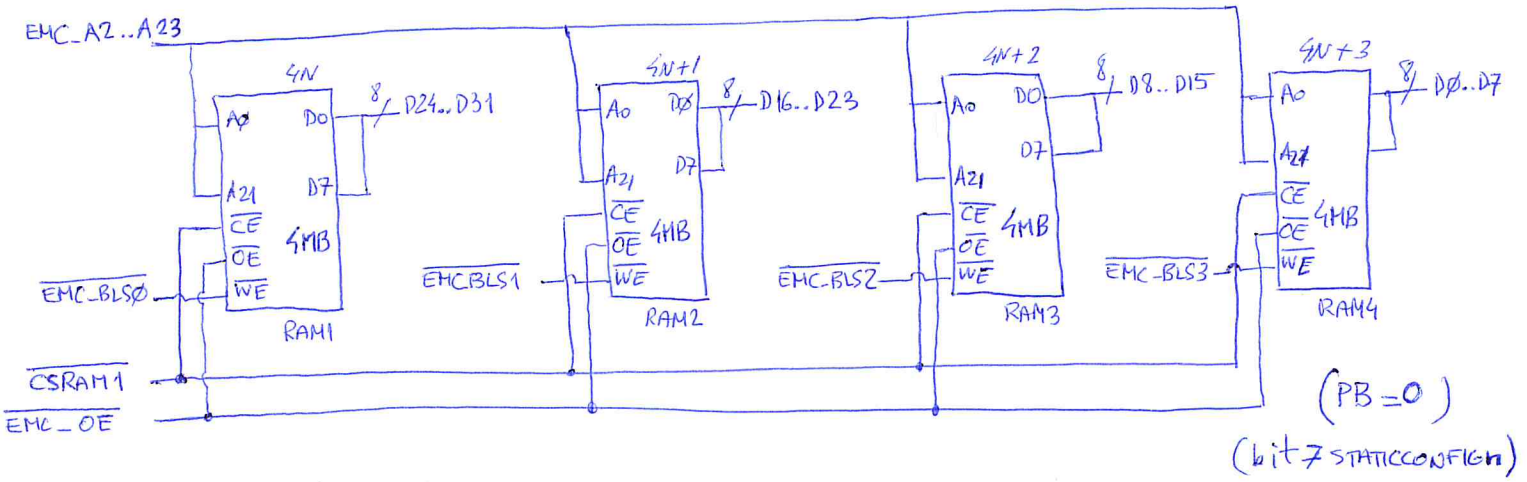
EJERCICIO 3

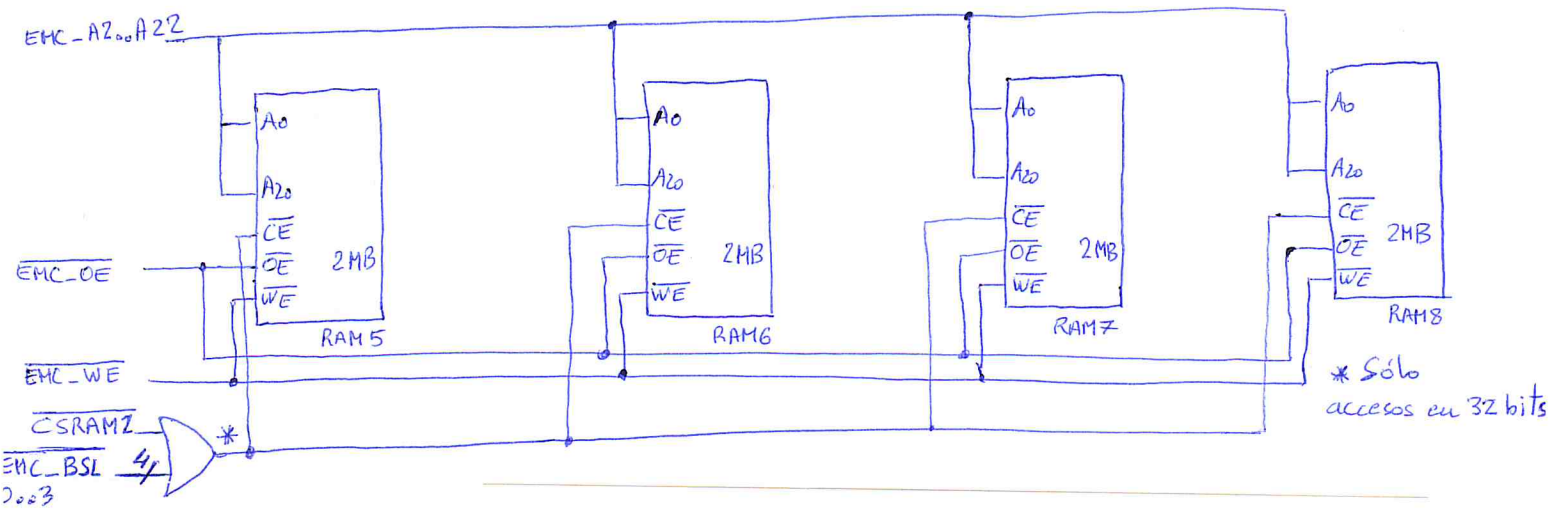
LPC1788 → BIG ENDIAN!.
Dispositivos de 8 bits

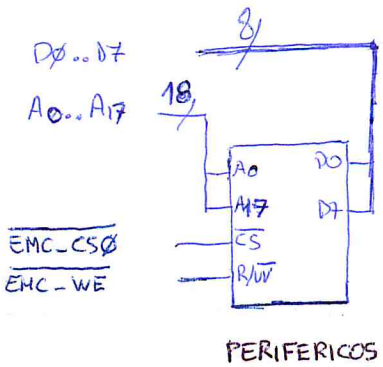
Caso 2

- 16 MB de SRAM con accesos en tamaño 8, 16 y 32 bits.
- 8 MB " " " " " " 32 bits.
- 256KB periféricos " " " " 8 bits.

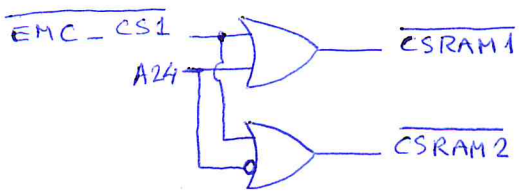
$\overline{EMC\_CS1}$ → 0x9000.0000 → SRAM → Ancho de bus 32 bits → STATICCONFIG1 (MW=0)
$\overline{EMC\_CS0}$ → 0x8000.0000 → PERIF. → " " " 8 bits → STATICCONFIG0 (MW=0)







DIRECCIONES	
0x9000.0000 0x90FF.FFFF	RAM1 4 x (4M x 8)
0x9100.0000 0x917F.FFFF	RAM2 4 x (2M x 8)



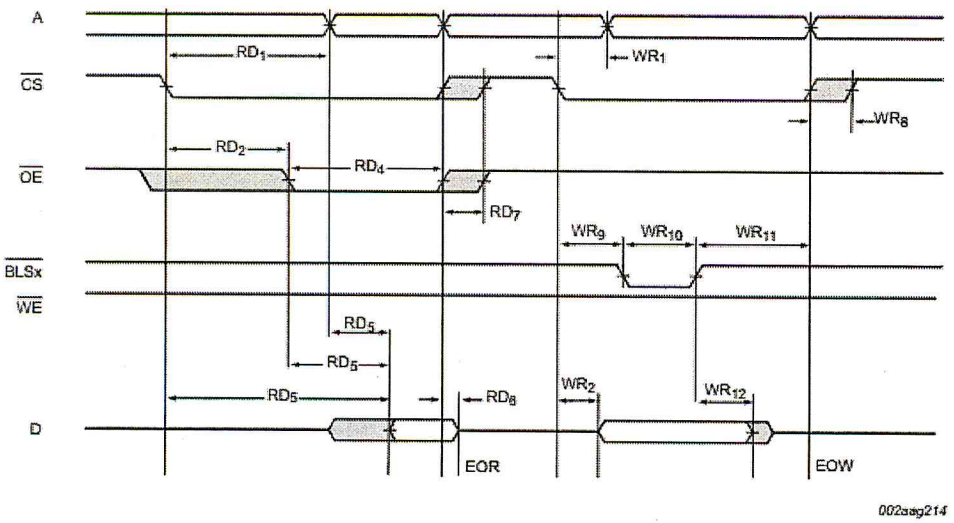


Fig 16. External static memory read/write access (PB = 0)

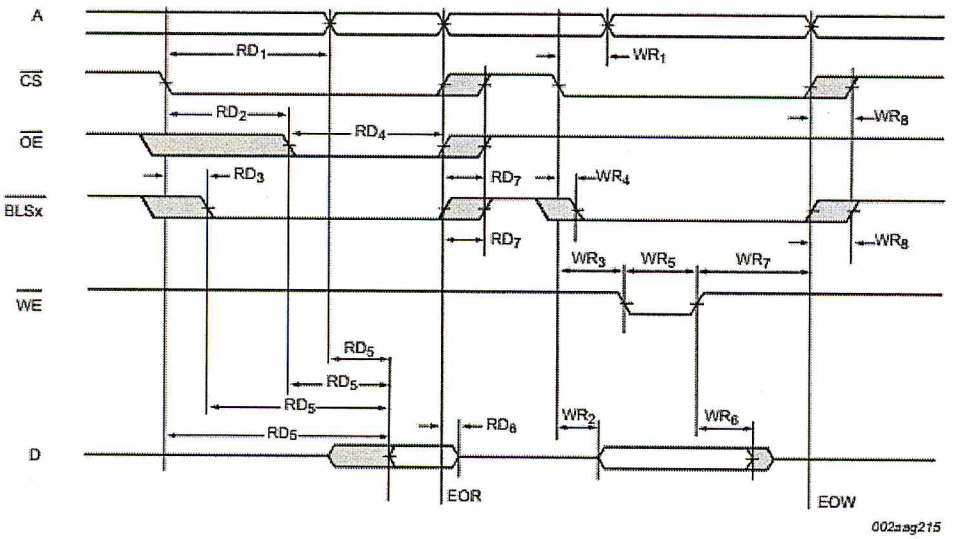


Fig 17. External static memory read/write access (PB =1)

Table 134. Static Memory Configuration registers (STATICCONFIG[0:3], address 0x2009 C200 (STATICCONFIG0), 0x2009 C220 (STATICCONFIG1), 0x2009 C240 (STATICCONFIG2), 0x2009 C260 (STATICCONFIG3)) bit description

Bit	Symbol	Value	Description	Reset Value
1:0	MW		Memory width.	0
		0x0	8 bit (POR reset value).	
		0x1	16 bit.	
		0x2	32 bit.	
		0x3	Reserved.	
2	-		Reserved. Read value is undefined, only zero should be written.	NA
3	PM		Page mode. In page mode the EMC can burst up to four external accesses. Therefore devices with asynchronous page mode burst four or higher devices are supported. Asynchronous page mode burst two devices are not supported and must be accessed normally.	0
		0	Disabled (POR reset value).	
		1	Asynchronous page mode enabled (page length four).	
5:4	-		Reserved. Read value is undefined, only zero should be written.	NA
6	PC		Chip select polarity. The value of the chip select polarity on power-on reset is 0.	0
		0	Active LOW chip select.	
		1	Active HIGH chip select.	
7	PB		Byte lane state. The byte lane state bit, PB, enables different types of memory to be connected. For byte-wide static memories the $\overline{BLS3:0}$ signal from the EMC is usually connected to $\overline{WE}$ (write enable). In this case for reads all the $\overline{BLS3:0}$ bits must be HIGH. This means that the byte lane state (PB) bit must be LOW. 16 bit wide static memory devices usually have the $\overline{BLS3:0}$ signals connected to the UBn and LBn (upper byte and lower byte) signals in the static memory. In this case a write to a particular byte must assert the appropriate UBn or LBn signal LOW. For reads, all the $\overline{UB}$ and $\overline{LB}$ signals must be asserted LOW so that the bus is driven. In this case the byte lane state (PB) bit must be HIGH.	0
		0	For reads all the bits in $\overline{BLS3:0}$ are HIGH. For writes the respective active bits in $\overline{BLS3:0}$ are LOW (POR reset value).	
		1	For reads the respective active bits in $\overline{BLS3:0}$ are LOW. For writes the respective active bits in $\overline{BLS3:0}$ are LOW.	