UNIVERSIDAD DE ALCALÁ ESCUELA POLITÉCNICA SUPERIOR DEPARTAMENTO DE ELECTRÓNICA		GRADO EN INGENIERÍA ELECTRÓNICA Y AUTOMÁTICA INDUSTRIAL	
ASIGNATURA	SISTEMAS ELECTRÓNICOS DIGITALES	CURSO	2014-2015
APELLIDOS, NOMBRE	SOLUCIÓN	DNI/GRUPO	

ENTREGABLE TEMA 4

Memorias SDRAM, DUAL-PORT

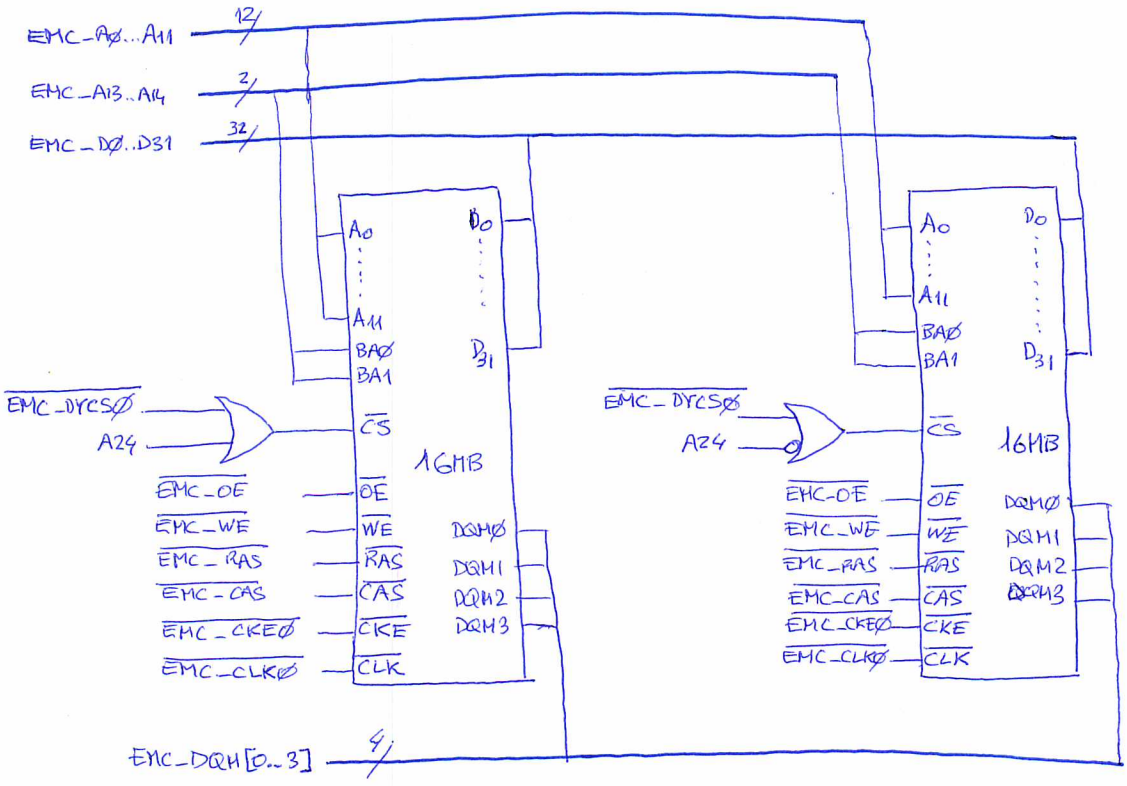
a) A partir del esquema del sistema de memoria de la tarjeta MYD-LPC1788 (ver hoja final):

1. Indique la capacidad y organización de la memoria SDRAM, así como el rango de direccionamiento dentro del mapa.

K4S561632D → 4M x 16bit x 4 bancos → 256 Mb → 32 Mbytes

$\overline{\text{EMC\_DYCS0}}$ → 0xA000.0000 – 0xA1FF.FFFF

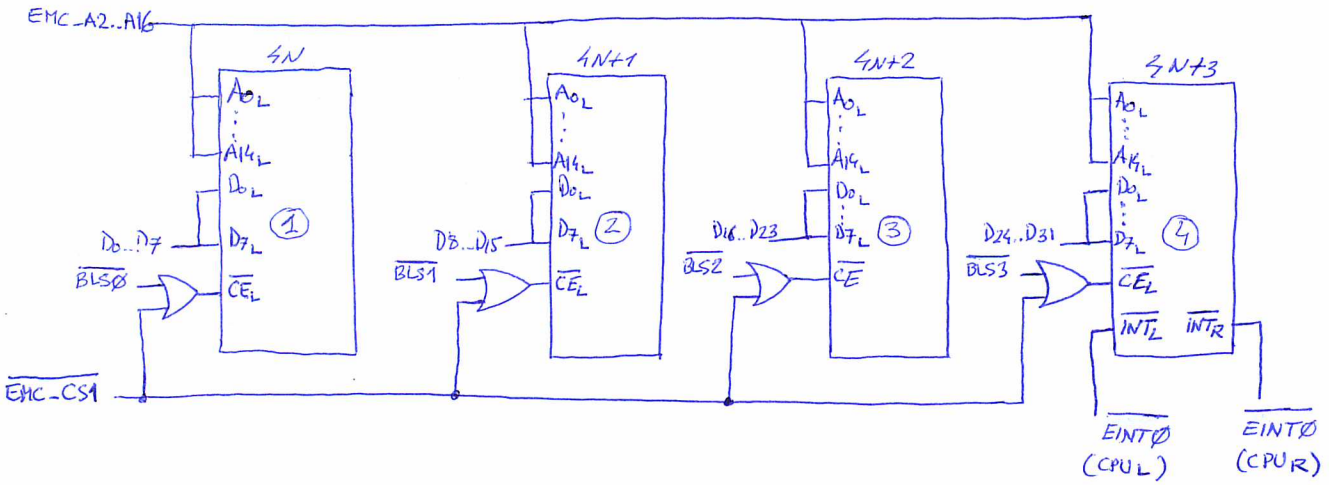
2. Proponga la solución para sustituir la SDRAM de 16 bits a partir del chip MT48LC4M32B2. Dibuje el nuevo diagrama de interconexión con el EMC del LPC1788 de forma simplificada (utilice buses para direcciones y datos) ignorando todas las señales de alimentación.



MT48LC4M32B2 → 1M x 32 x 4 bancos → 16 Mbytes

b) Se desea añadir 128Kbytes de memoria Dual-Port a partir del chip CY70xxAV con objeto de poder compartir esta memoria con un segundo LPC1788 en modo 32bits. Dibuje de forma simplificada el diagrama de interconexión de la memoria Dual-Port (lado L) resultante con el EMC del LPC1788 base de la tarjeta. Considere que la arbitración se realiza por interrupción utilizando el lado L la última dirección de memoria impar. Explique brevemente su funcionamiento a partir de la solución adoptada.

CY7C007 → 32K×8 (4 chips)



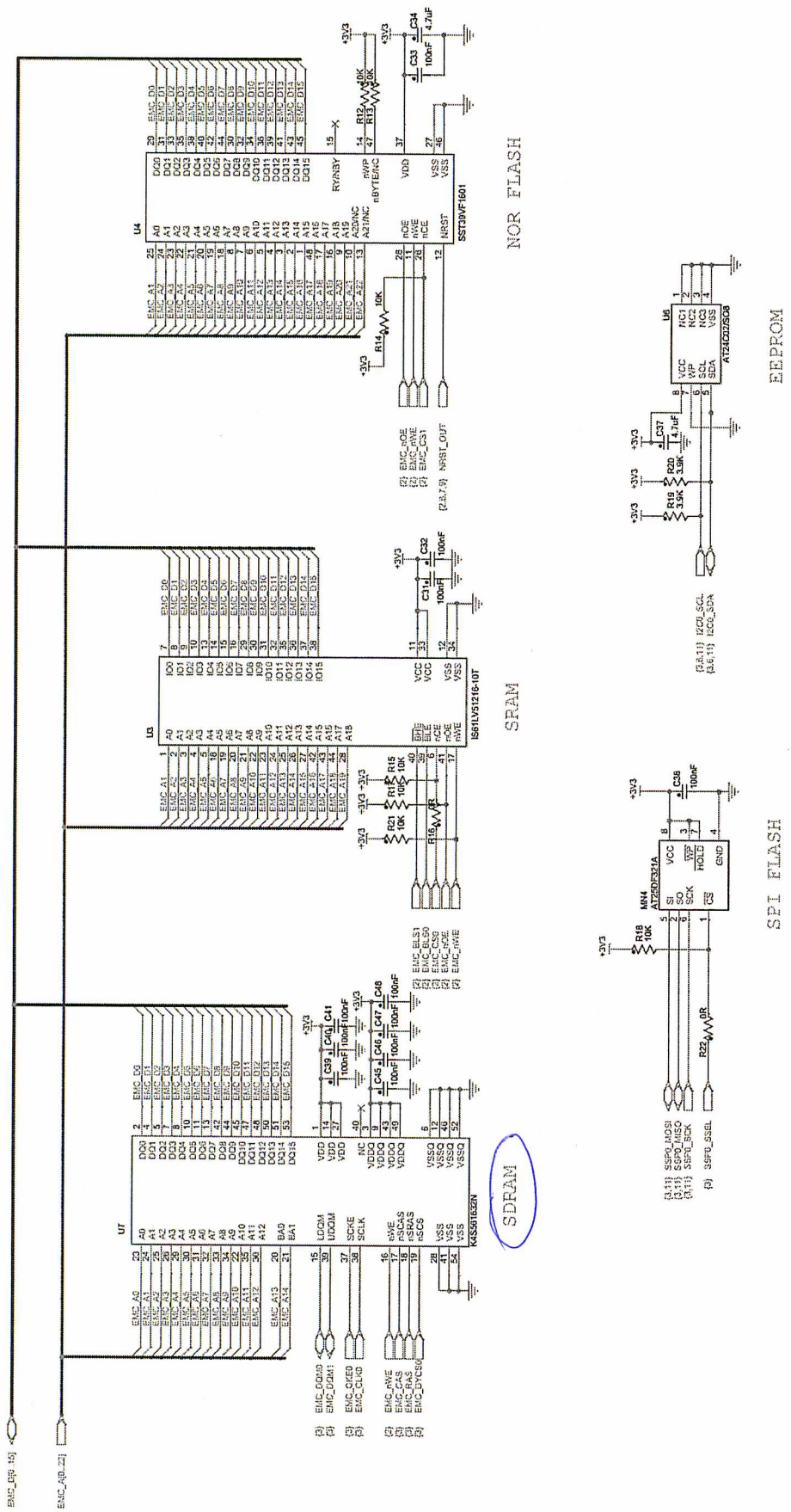
DIR. arbitración CPU_L { Øx9001.FFFF (última chip 4) ; Øx9001.FFFB (penúltima chip 4)

CPU_L escribe en Øx9001.FFFF → $\overline{EINT0}$ = Ø (CPU_R) → Activa int. externa

CPU_R lee en Øx9001.FFFF → $\overline{EINT0}$ = 1 (CPU_R) → Desactiva " "

CPU_R escribe en Øx9001.FFFB → $\overline{EINT0}$ = Ø (CPU_L) → Activa int. externa

CPU_L lee en Øx9001.FFFB → $\overline{EINT0}$ = 1 (CPU_L) → Desact. " "


NOR FLASH
SRAM
SDRAM
SPI FLASH
EEPROM

4M x 16Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (8K Cycle)

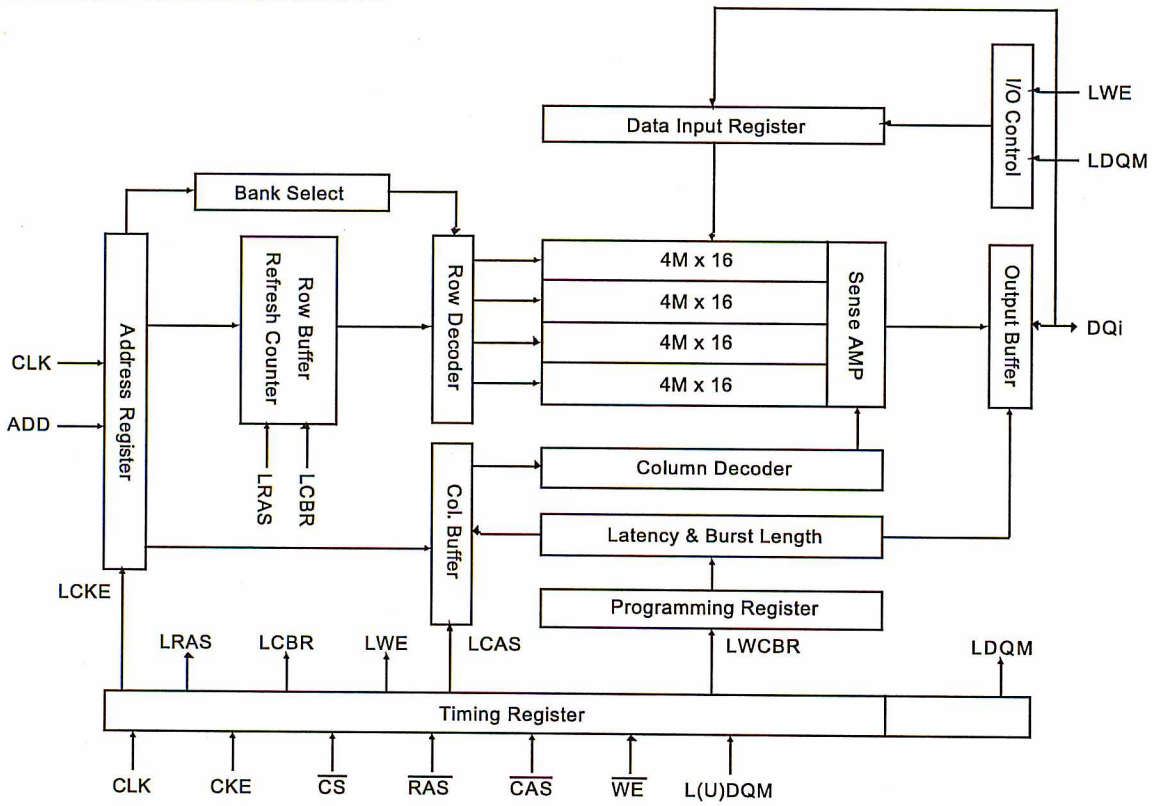
GENERAL DESCRIPTION

The K4S561632D is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 4,196,304 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S561632D-TC/L60	166MHz(CL=3)	LVTTL	54pin TSOP(II)
K4S561632D-TC/L7C	133MHz(CL=2)		
K4S561632D-TC/L75	133MHz(CL=3)		
K4S561632D-TC/L1H	100MHz(CL=2)		
K4S561632D-TC/L1L	100MHz(CL=3)		

FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

SDR SDRAM

MT48LC4M32B2 – 1 Meg x 32 x 4 Banks

Features

- PC100-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh mode (not available on AT devices)
- Auto refresh
  - 64ms, 4096-cycle refresh (commercial and industrial)
  - 16ms, 4096-cycle refresh (automotive)
- LVTTL-compatible inputs and outputs
- Single 3.3V ±0.3V power supply
- Supports CAS latency (CL) of 1, 2, and 3

Options	Marking
• Configuration	
– 4 Meg x 32 (1 Meg x 32 x 4 banks)	4M32B2
• Package – OCPL[1]	
– 86-pin TSOP II (400 mil)	TG
– 86-pin TSOP II (400 mil) Pb-free	P
– 90-ball VFBGA (8mm x 13mm)	F5
– 90-ball VFBGA (8mm x 13mm) Pb-free	B5
• Timing (cycle time)	
– 6ns (166 MHz)	-6A[2]
– 6ns (166 MHz)	-6[3]
– 7ns (143 MHz)	-7[3]
• Revision	:G/:L
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
– Automotive (–40°C to +105°C)	AT[4]

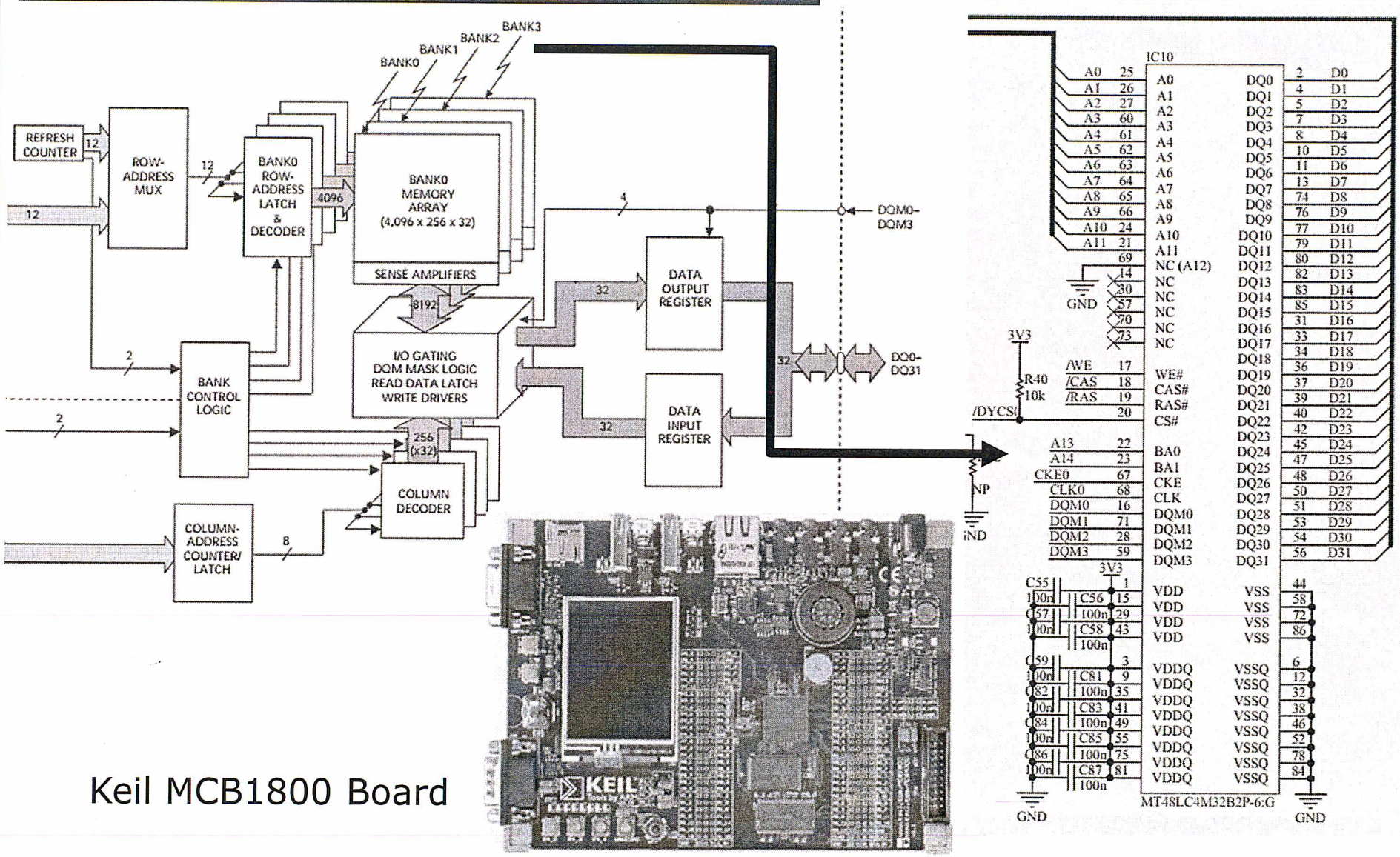
Notes:
1. Off-center parting line.
2. Available only on Revision L.
3. Available only on Revision G.
4. Contact Micron for availability.

Table 1: Key Timing Parameters

CL = CAS (READ) latency

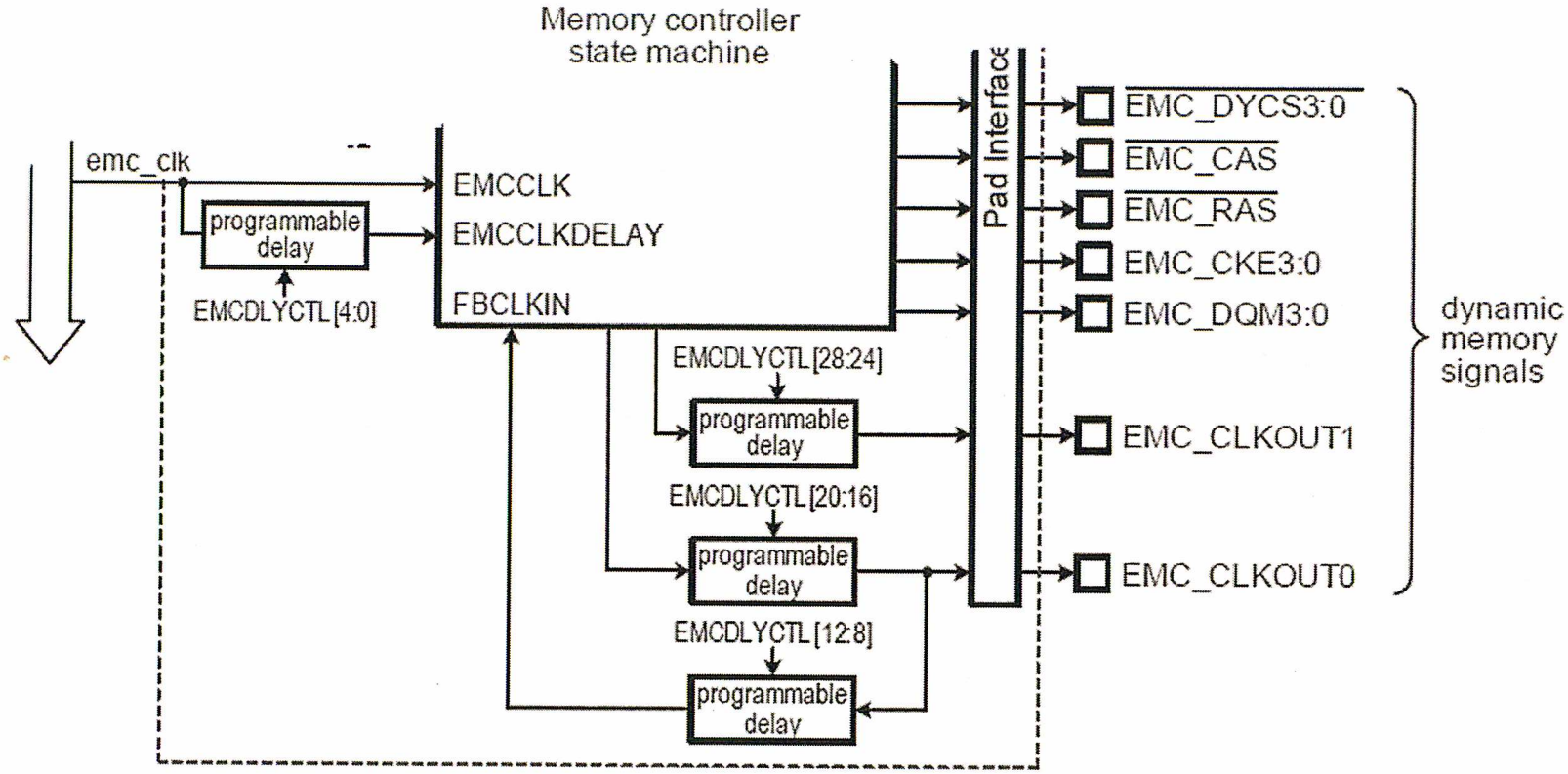
Speed Grade	Clock Frequency (MHz)	Target tRCD-tRP-CL	tRCD (ns)	tRP (ns)	CL (ns)
-6A	167	3-3-3	18	18	18
-6	167	3-3-3	18	18	18
-7	143	3-3-3	20	20	21

4.3. EMC: SDRAM connection example



Keil MCB1800 Board

4.3. LPC178x: SDRAM signals of EMC



Chip select pin	Address range	Memory type	Size of range
EMC_$\overline{\text{DYCS0}}$	0xA000 0000 - 0xAFFF FFFF	Dynamic	256 MB
EMC_$\overline{\text{DYCS1}}$	0xB000 0000 - 0xBFFF FFFF	Dynamic	256 MB
EMC_$\overline{\text{DYCS2}}$	0xC000 0000 - 0xCFFF FFFF	Dynamic	256 MB
EMC_$\overline{\text{DYCS3}}$	0xD000 0000 - 0xDFFF FFFF	Dynamic	256 MB