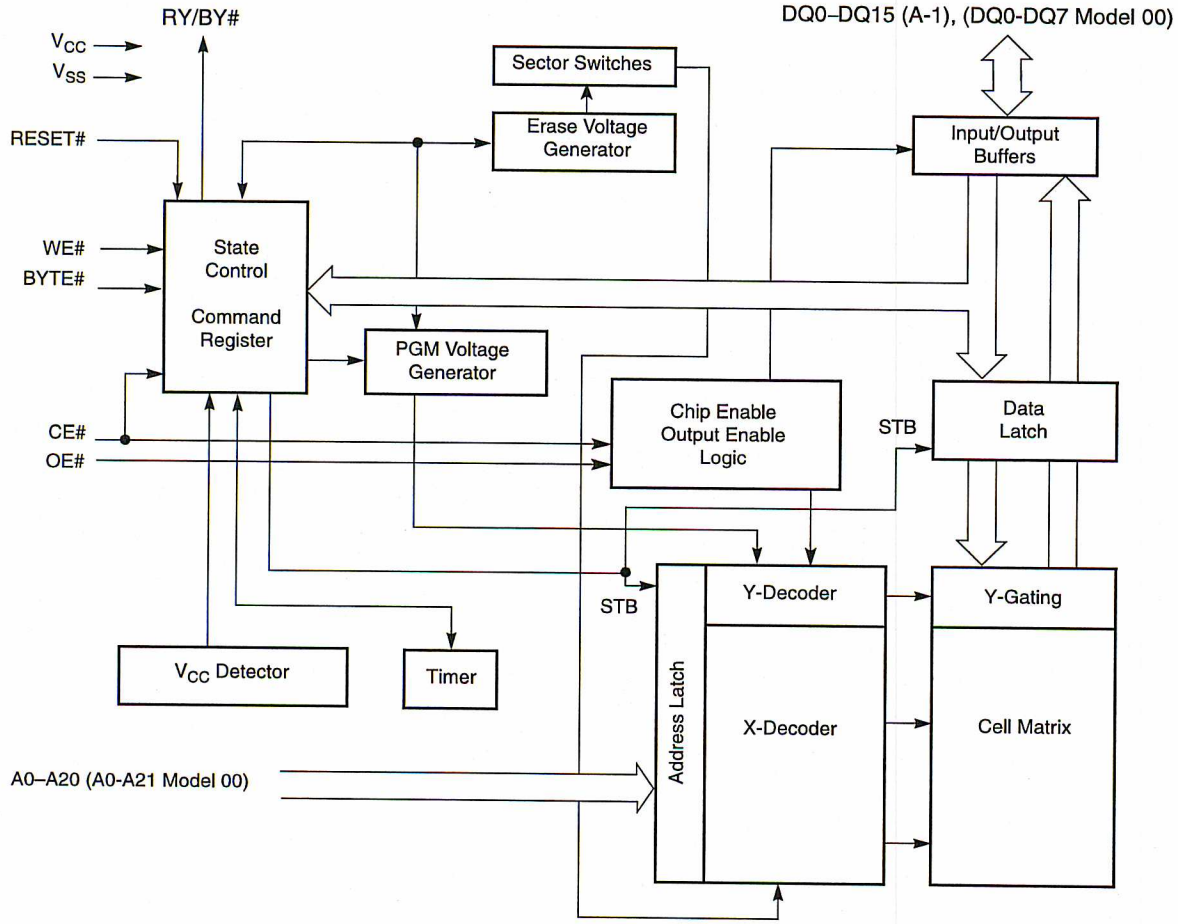
29AL032D (32Mbits)
4M×8 / 2M×16

1. Product Selector Guide

Family Part Number		S29AL032D	
Speed Option	Voltage Range: V_{CC} = 2.7–3.6 V	70	90
Max access time, ns (t_{ACC})		70	90
Max CE# access time, ns (t_{CE})		70	90
Max OE# access time, ns (t_{OE})		30	35

Note
See AC Characteristics on page 49 for full specifications.

2. Block Diagram

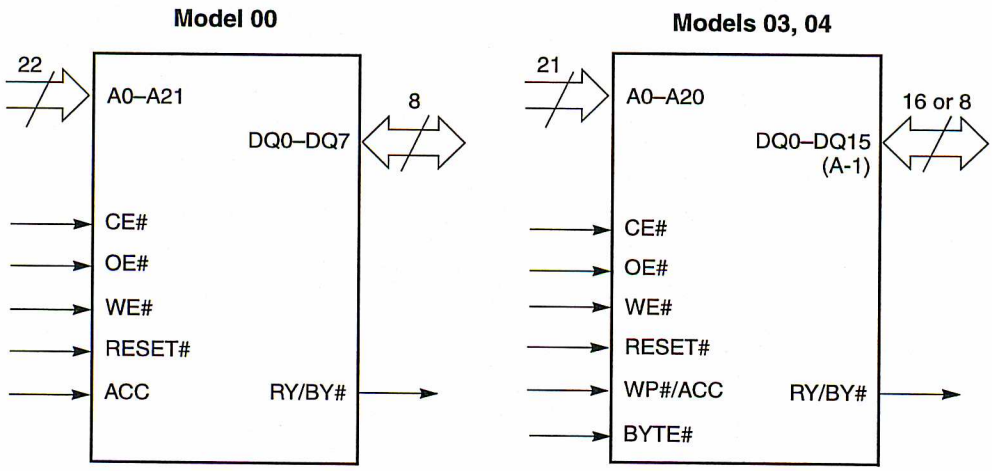


4. Pin Configuration

Pin	Description
A0–A21	22 address inputs
A0-A20	21 address inputs
DQ0–DQ7	8 data inputs/outputs
DQ0-DQ14	15 data inputs/outputs
DQ15/A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	Selects 8-bit or 16-bit mode
CE#	Chip enable
OE#	Output enable
WE#	Write enable
RESET#	Hardware reset pin
WP#/ACC	Hardware Write Protect input/Programming Acceleration input.
ACC	Hardware Write Protect input
RY/BY#	Ready/Busy output
V_{CC}	3.0 volt-only single power supply (see Product Selector Guide on page 6 for speed options and voltage supply tolerances)
V_{SS}	Device ground
NC	Pin not connected internally

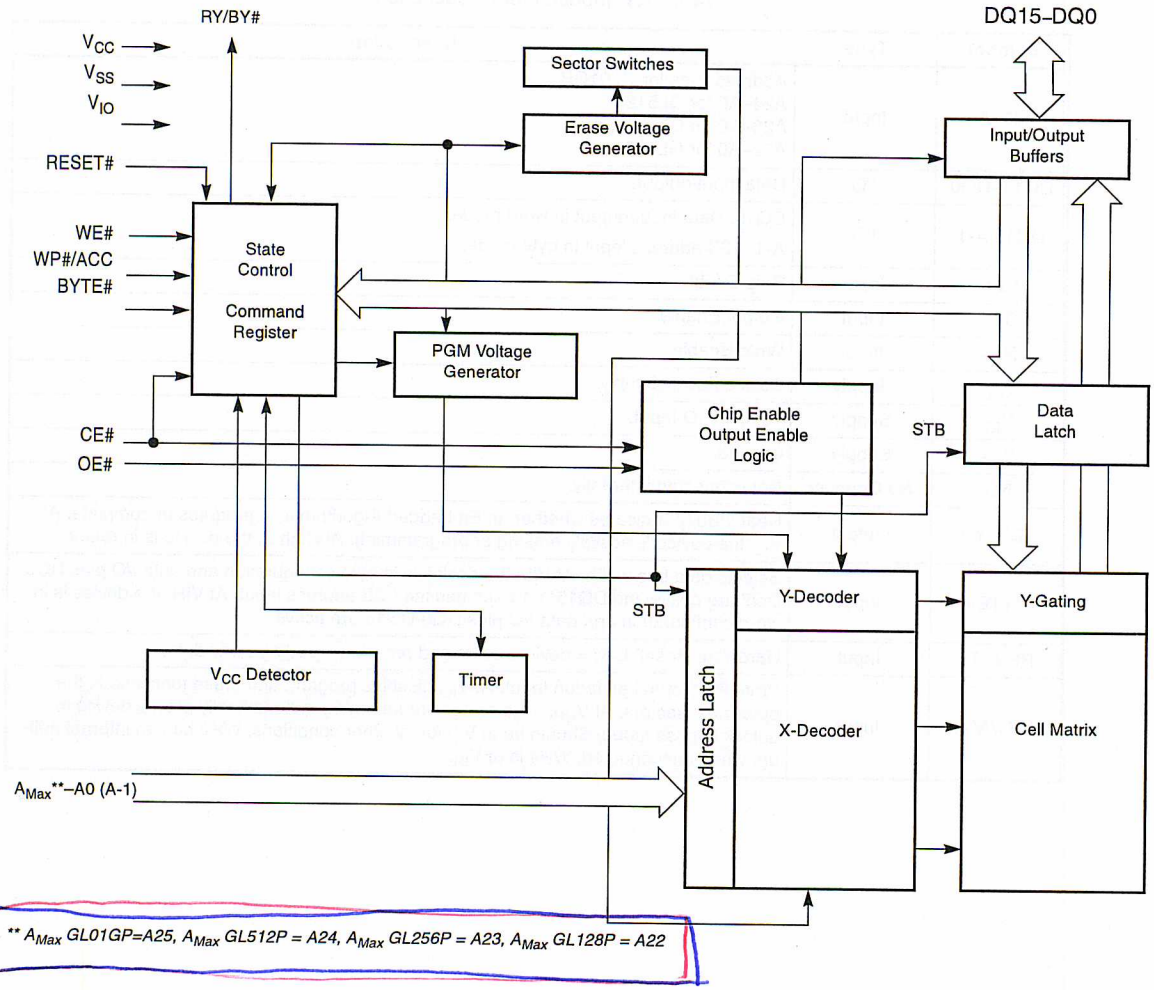
5. Logic Symbols

Figure 5.1 Logic Symbols



3. Block Diagram

Figure 3.1 S29GL-P Block Diagram



4. Physical Dimensions/Connection Diagrams

This section shows the I/O designations and package specifications for the S29GL-P family.

4.1 Related Documents

The following documents contain information relating to the S29GL-P devices. Click on the title or go to www.spansion.com download the PDF file, or request a copy from your sales office.

- Considerations for X-ray Inspection of Surface-Mounted Flash Integrated Circuits

4.2 Special Handling Instructions for BGA Package

Special handling is required for Flash Memory products in BGA packages.

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

2. Input/Output Descriptions & Logic Symbol

Table 2.1 identifies the input and output package connections provided on the device.

Table 2.1 Input/Output Descriptions

Symbol	Type	Description
A25–A0	Input	Address lines for GL01GP A24–A0 for GL512P A23–A0 for GL256P, A22–A0 for GL128P.
DQ14–DQ0	I/O	Data input/output.
DQ15/A-1	I/O	DQ15: Data input/output in word mode. A-1: LSB address input in byte mode.
CE#	Input	Chip Enable.
OE#	Input	Output Enable.
WE#	Input	Write Enable.
V_{CC}	Supply	Device Power Supply.
V_{IO}	Supply	Versatile IO Input.
V_{SS}	Supply	Ground.
NC	No Connect	Not connected internally.
RY/BY#	Output	Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively erasing or programming. At High Z, the device is in ready.
BYTE#	Input	Selects data bus width. At VIL, the device is in byte configuration and data I/O pins DQ0-DQ7 are active and DQ15/A-1 becomes the LSB address input. At VIH, the device is in word configuration and data I/O pins DQ0-DQ15 are active.
RESET#	Input	Hardware Reset. Low = device resets and returns to reading array data.
WP#/ACC	Input	Write Protect/Acceleration Input. At V_{IL}, disables program and erase functions in the outermost sectors. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. Should be at V_{IH} for all other conditions. WP# has an internal pull-up; when unconnected, WP# is at V_{IH}.

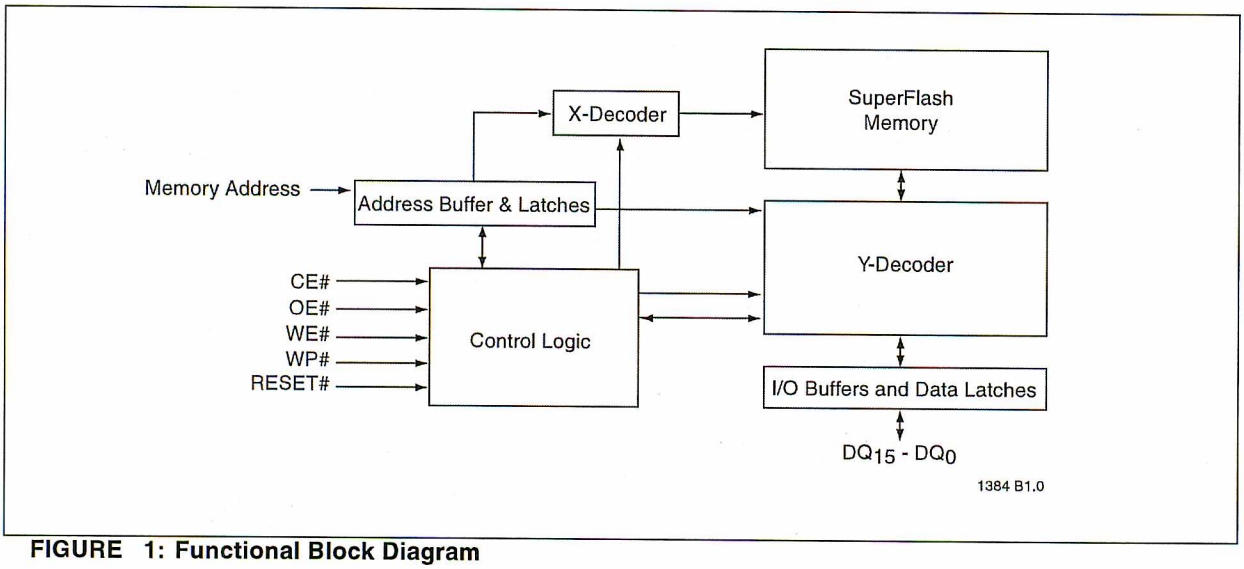


FIGURE 1: Functional Block Diagram

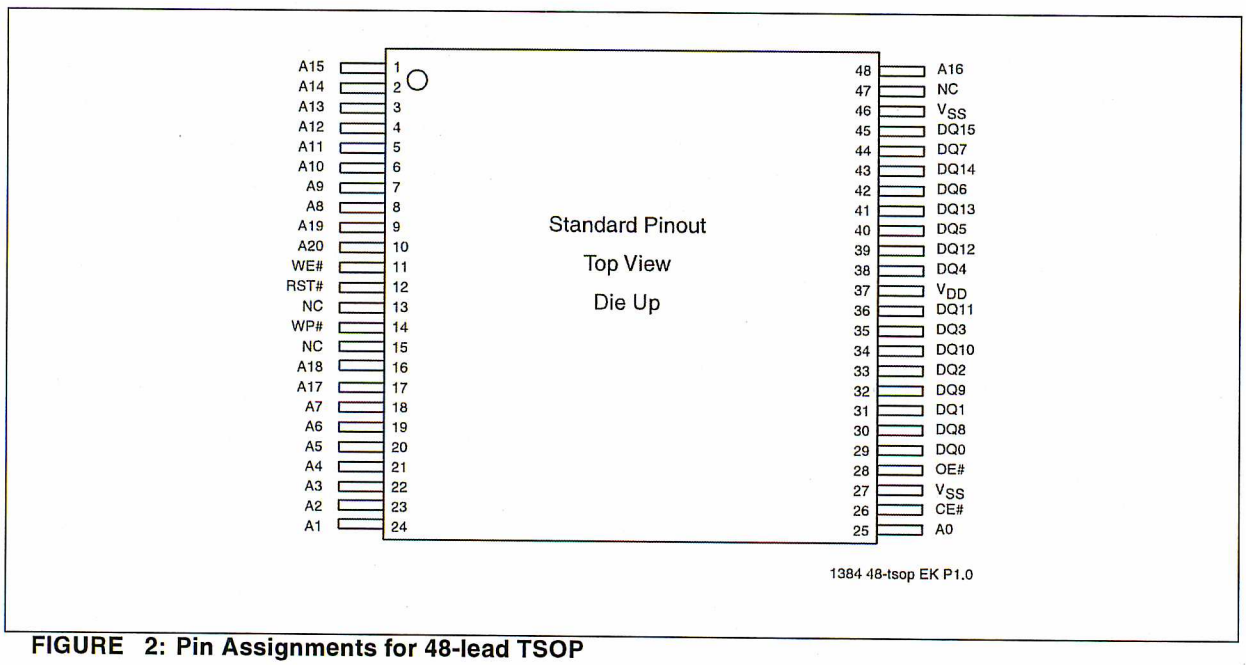


FIGURE 2: Pin Assignments for 48-lead TSOP

IS65WV25616ALL
IS65WV25616BLL

ISSI®

256K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC SRAM

PRELIMINARY INFORMATION
JUNE 2006

FEATURES

- High-speed access time: 55ns, 70ns
- CMOS low power operation
  36 mW (typical) operating
  9 µW (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  1.65V--2.2V V_{DD} (65WV25616ALL)
  2.5V--3.6V V_{DD} (65WV25616BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- TEMPERATURE OFFERINGS:
  Option A1: -40°C to +85°C
  Option A2: -40°C to +105°C
  Option A3: -40°C to +125°C
- Lead-free available

DESCRIPTION

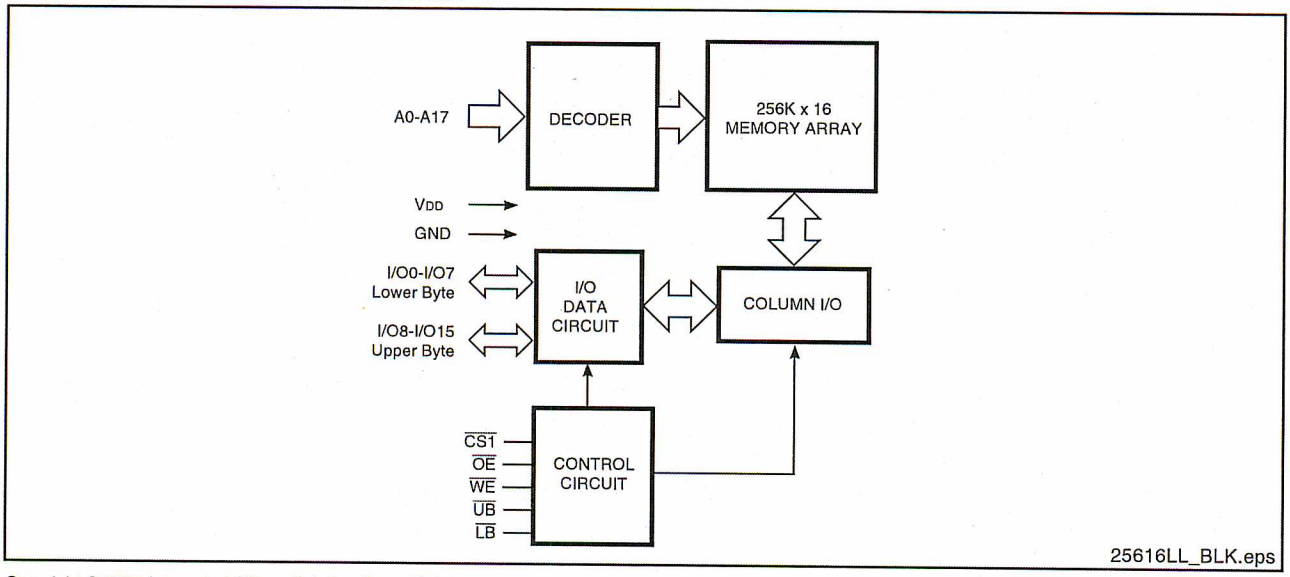
The *ISSI* IS65WV25616ALL/IS65WV25616BLL are high-speed, low power, 4M bit SRAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when $\overline{CS1}$ is LOW, and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS65WV25616BALL/65WV25616BLL are packaged in the JEDEC standard 44-Pin TSOP (TYPE II).

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY

16Mbit CMOS SRAM

3DS16-325

512K x 32 Bit High-Speed CMOS Static RAM-5.0V Operating

FEATURES

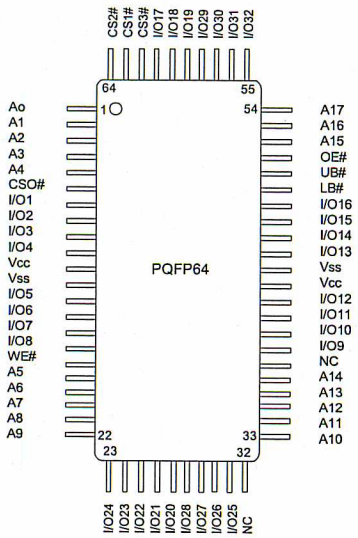
- Fast Access Time : 15 or 20ns
- Single 5.0 ± 0.5V Power Supply
- Power Dissipation
  - Standby 80mA
  - Operating 540mA (Max.)
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Die Control : CS0#, CS1#, CS2# and CS3# chip select

DESCRIPTION

The 3DS16-325 is a 16,777,216 - bit high-speed Static Random Access Memory organized as 4 banks of 262,144 words of 16 bits. Two banks can operate silmultaneously, giving 32 bit processing. The 3DS16-325 uses 32 common input and output lines and has an output enable pin which operates faster than address access time at read cycle.
Also it allows lower and upper byte access by data control (UB#, LB#). The device is manufactured using 3D PLUS well known MCM-V patended technology designed for high-speed circuit applications. It is particularly well suited for use in high-density high-speed system applications. The 3DS16-325 is packaged in a 64-pin PQFP.

PIN CONFIGURATION

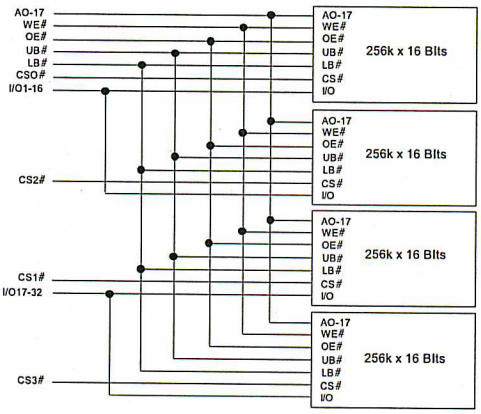
3DS16-325S (TOP VIEW)



PIN DESCRIPTION

A0-A17	Address Inputs
WE#	Write Enable
CS0#, CS1# CS2#, CS3#	Chip Selects
OE#	Output Enable
LB#	Lower - Byte Control
UB#	Upper - Byte Control
I/O1 - I/O32	Data Inputs / Outputs
Vcc	5.0 V Power
Vss	Ground
NC	No Connection

BLOCK DIAGRAM



3D PLUS, 641 rue Hélène Boucher - ZI
F-78532 BUC Cedex FRANCE
Tel : 33 (0)1 30 83 26 50 FAX : 33 (0)1 39 56 25 89
Web : http://www. 3d-plus.com

CY7C1071DV33

32-Mbit (2 M × 16) Static RAM

Features

- High speed
  - t_{AA} = 12 ns
- Low active power
  - I_{CC} = 250 mA at 83.3 MHz
- Low Complementary Metal Oxide Semiconductor (CMOS) standby power
  - I_{SB2} = 50 mA
- Operating voltages of 3.3 ± 0.3 V
- 2.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Available in Pb-free 48-ball FBGA package

Functional Description

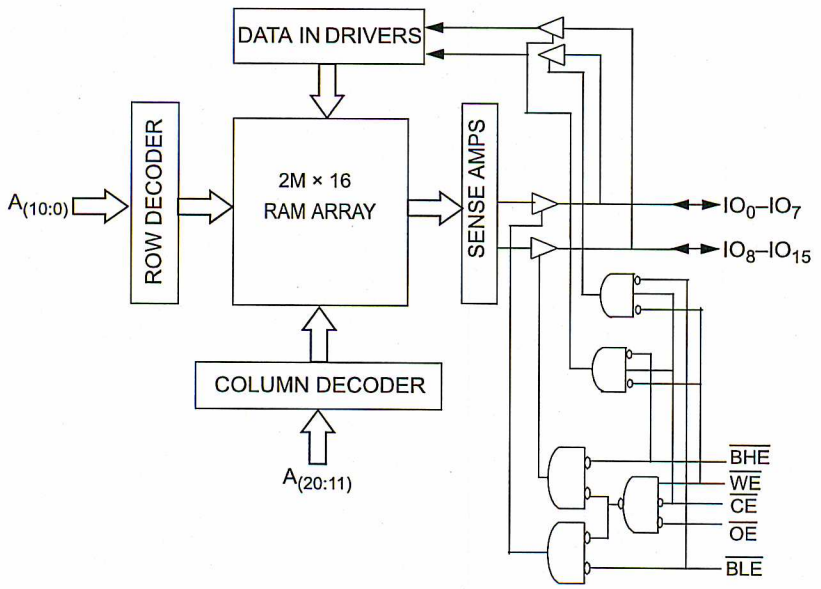
The CY7C1071DV33 is a high performance CMOS Static RAM organized as 2,097,152 words by 16 bits. The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when:

- Deselected ($\overline{CE}$ HIGH)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both byte high enable and byte low enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- The write operation is active ($\overline{CE}$ LOW and $\overline{WE}$ LOW)

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{20}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{20}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 10 for a complete description of read and write modes.

Logic Block Diagram



CY62128B MoBL®

128K x 8 Static RAM

Features

- **4.5V–5.5V operation**
- **CMOS for optimum speed/power**
- **Low active power (70 ns, LL version)**
  - **—82.5 mW (max.) (15 mA)**
- **Low standby power (70 ns, LL version)**
  - **—110 µW (max.) (15 µA)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options**

Functional Description

The CY62128B is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}_1$), an active HIGH Chip Enable (CE_2), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

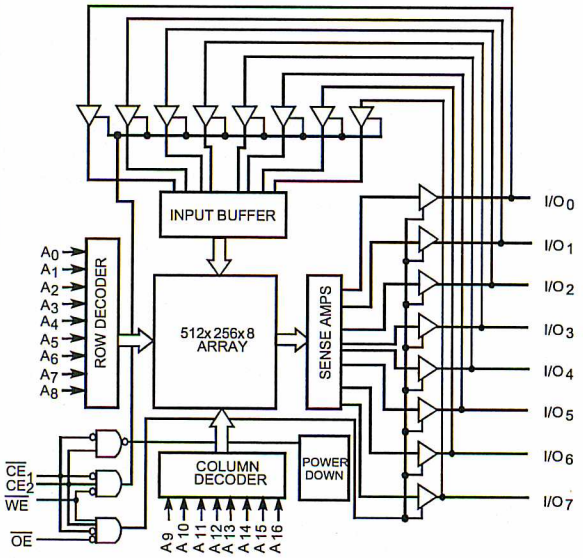
Writing to the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable Two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable Two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

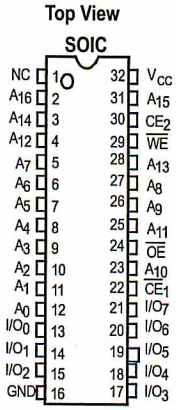
The CY62128B is available in a standard 450-mil-wide SOIC, 32-pin TSOP type I and STSOP packages.

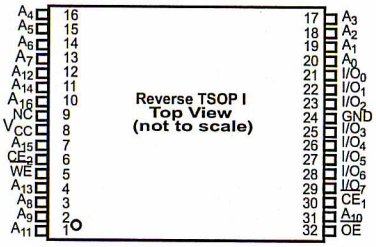
Logic Block Diagram

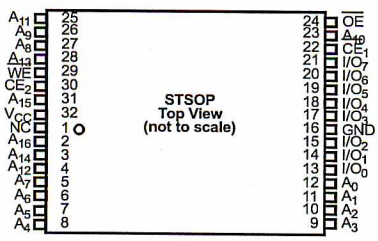


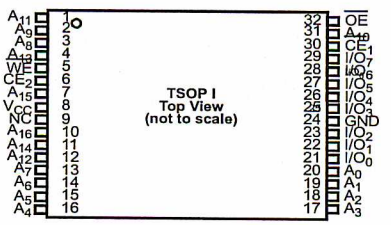
Pin Configurations

Top View
SOIC









SYNCHRONOUS DRAM

MT48LC8M32B2 - 2 Meg x 32 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/sdramds

FEATURES

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh (15.6µs/row)
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Supports CAS latency of 1, 2, and 3

OPTIONS

	MARKING
• Configuration	
8 Meg x 32 (2 Meg x 32 x 4 banks)	8M32B2
• Package	
86-pin TSOP (400 mil)	TG
86-pin TSOP (400 mil) Lead-free	P
90-ball FBGA (8mm x 13mm)	F5[1]
90-ball FBGA (8mm x 13mm) Lead-free	B5[1]
• Timing (Cycle Time)	
6ns (166 MHz)	-6
7ns (143 MHz)	-7
• Operating Temperature Range	
Commercial (0° to +70°C)	None
Industrial (-40°C to +85°C)	IT[1]

NOTE: 1. Available on -7 only

Part Number Example:
MT48LC8M32B2TG-7

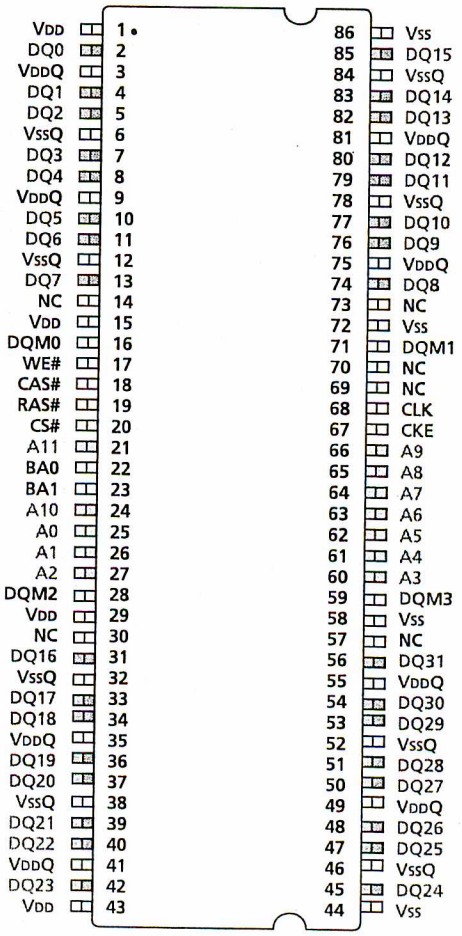
KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME CL = 3*	SETUP TIME	HOLD TIME
-6	166 MHz	5.5ns	1.5ns	1ns
-7	143 MHz	6.0ns	2ns	1ns

*CL = CAS (READ) latency

Pin Assignment (Top View)

86-Pin TSOP



Note: The # symbol indicates signal is active LOW.

	8 Meg x 32
Configuration	2 Meg x 32 x 4 banks
Refresh Count	4K
Row Addressing	4K (A0–A11)
Bank Addressing	4 (BA0, BA1)
Column Addressing	512 (A0–A8)

FUNCTIONAL BLOCK DIAGRAM
8 Meg x 32 SDRAM