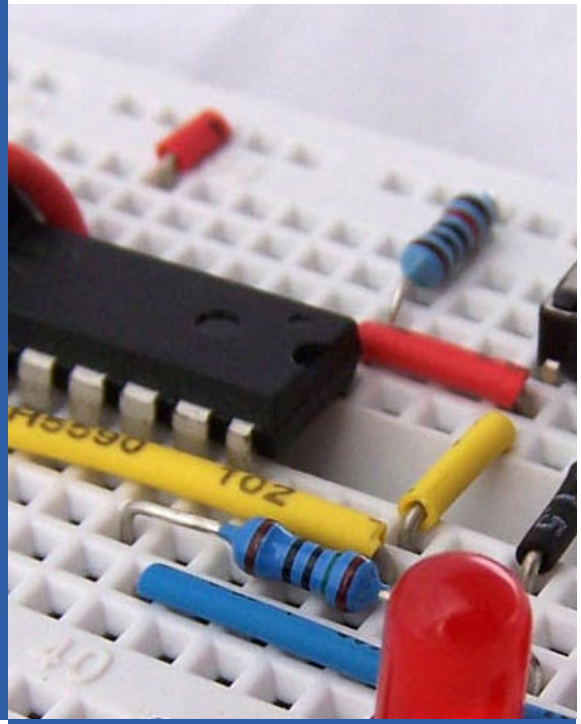
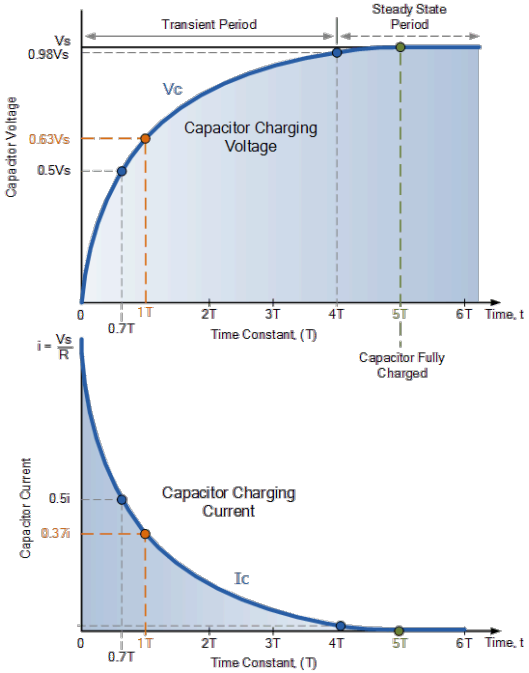
Electrónica y Tecnología de Computadores

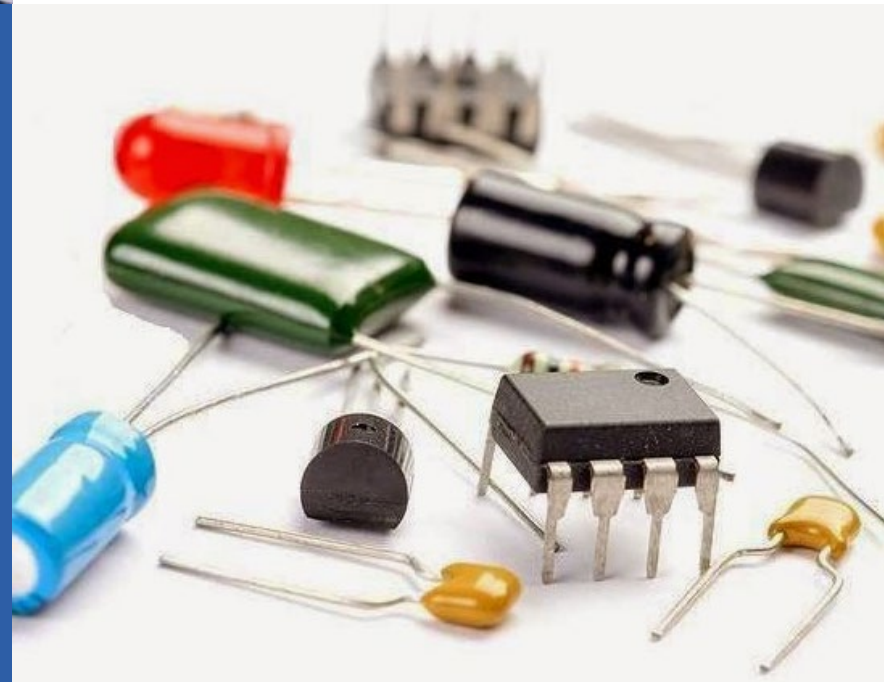


Universidad Francisco de Vitoria
UFV Madrid

TEMA 3
Electricidad y electromagnetismo

Semiconductores



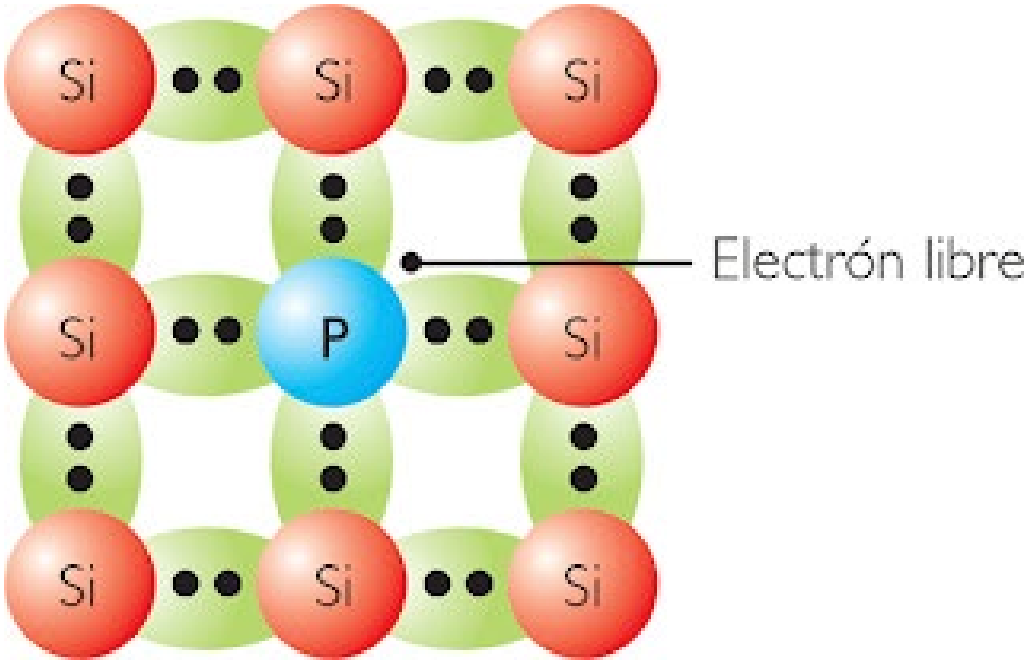


Introducción

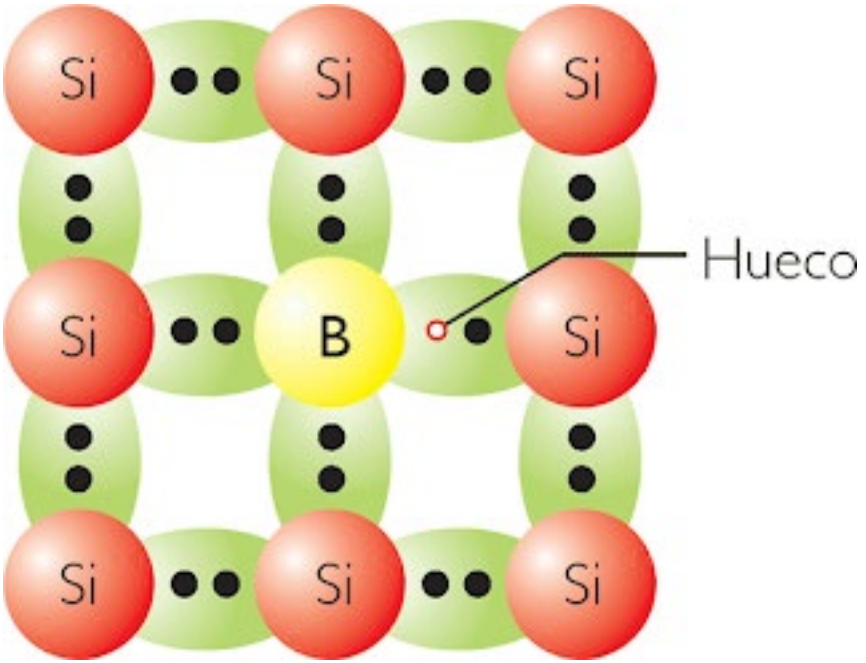
- En este apartado se presentan los semiconductores, materiales no óhmicos, que forman la base de la fabricación de puertas lógicas.
- Contenidos:
  - Materiales de tipo N y de tipo P
  - Uniones NP, barrera potencial (zona de deplexión)
  - Diodos en su modelo ideal y simplificado lineal
  - Transistores bipolares NPN y PNP
  - Transistores de efecto de campo (FET) canal N y canal P

- Este tema está fuertemente apoyado por los videos recomendados

Materiales de tipo N y de tipo P

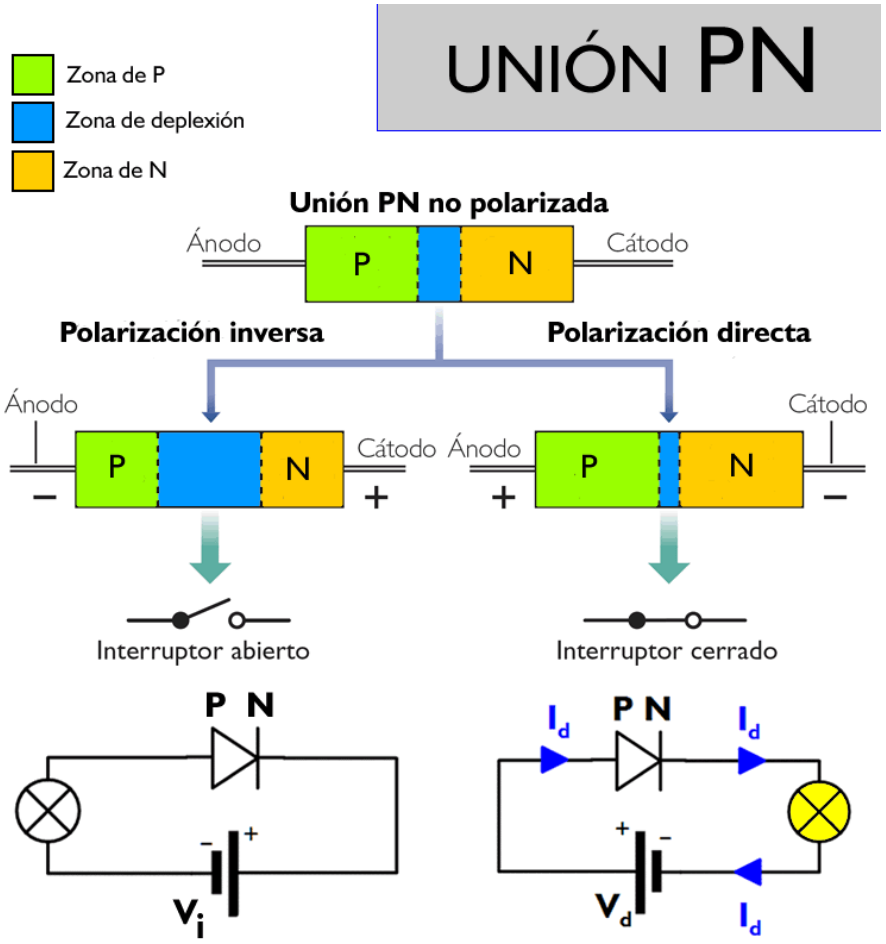


Tipo N
(dopaje fósforo)



Tipo P
(dopaje Boro)

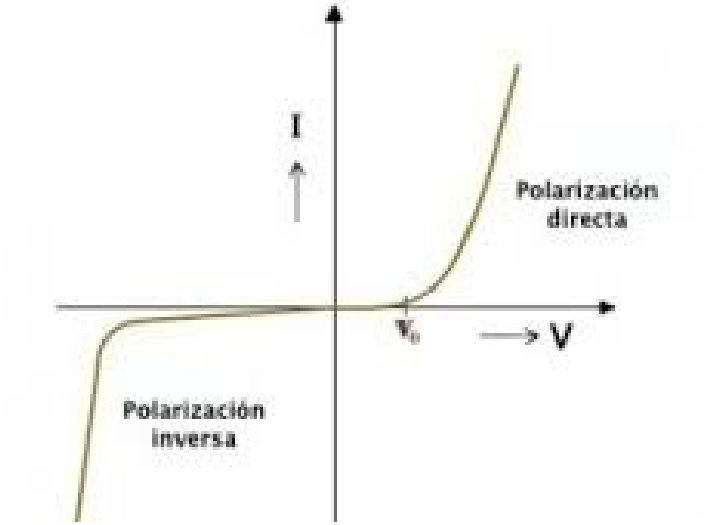
Uniones NP (o PN)



Barrera de voltaje o zona de deplexión

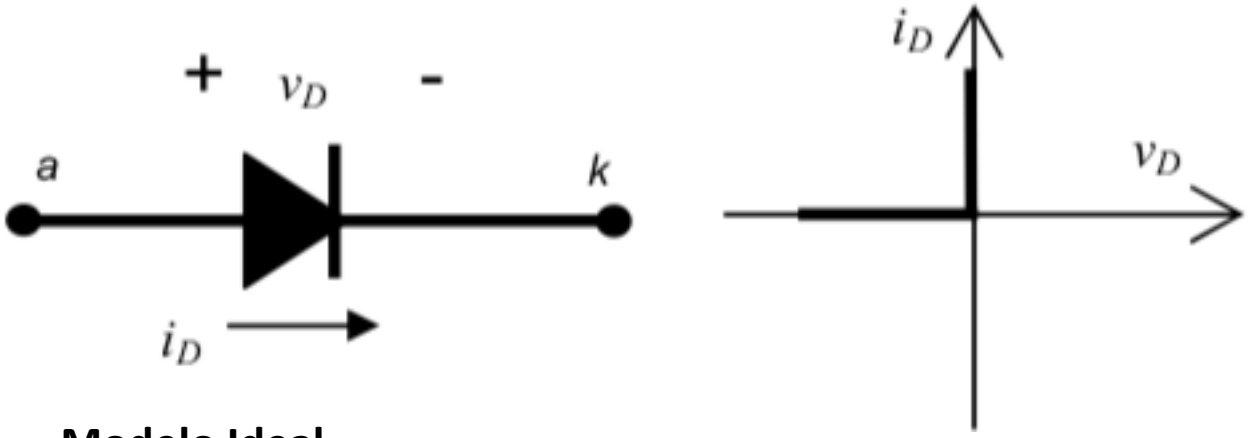
- Transmite en polarización directa
- Corta en polarización inversa
- Tiene zona de ruptura (avalancha)

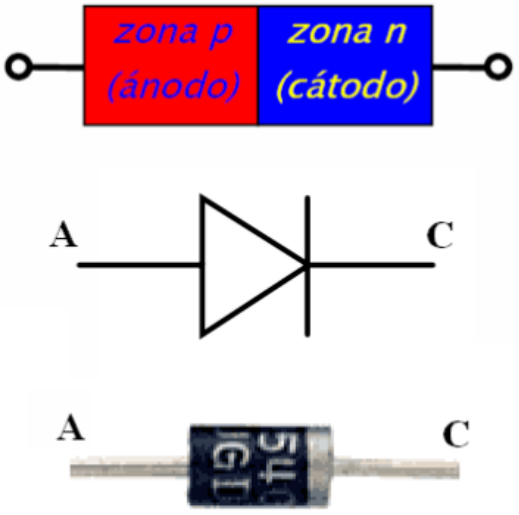
El diodo: Unión NP



Modelo Real

Polarización directa, Vo = 0,6..0,7 para silicio



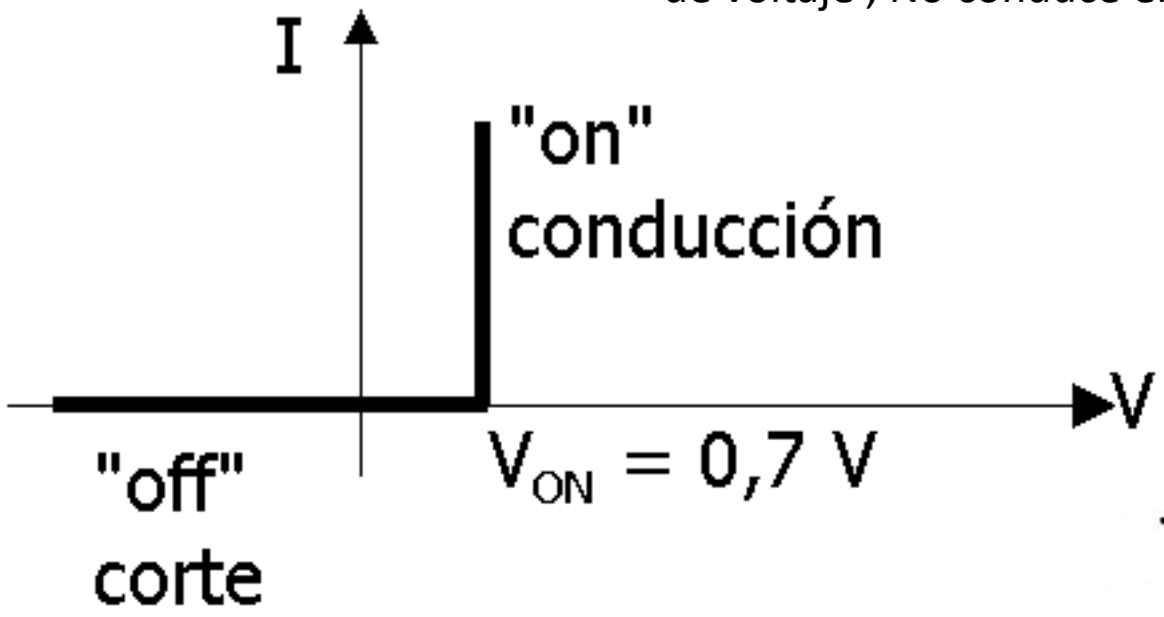


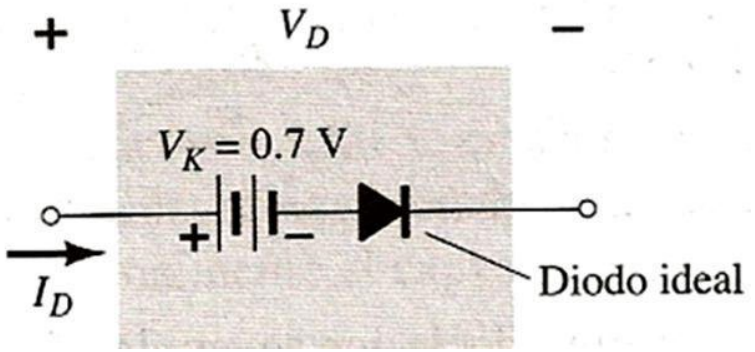
Modelo Ideal

Conduce en directa con R=0, No conduce en inversa

El diodo: Unión NP (Modelo simplificado)

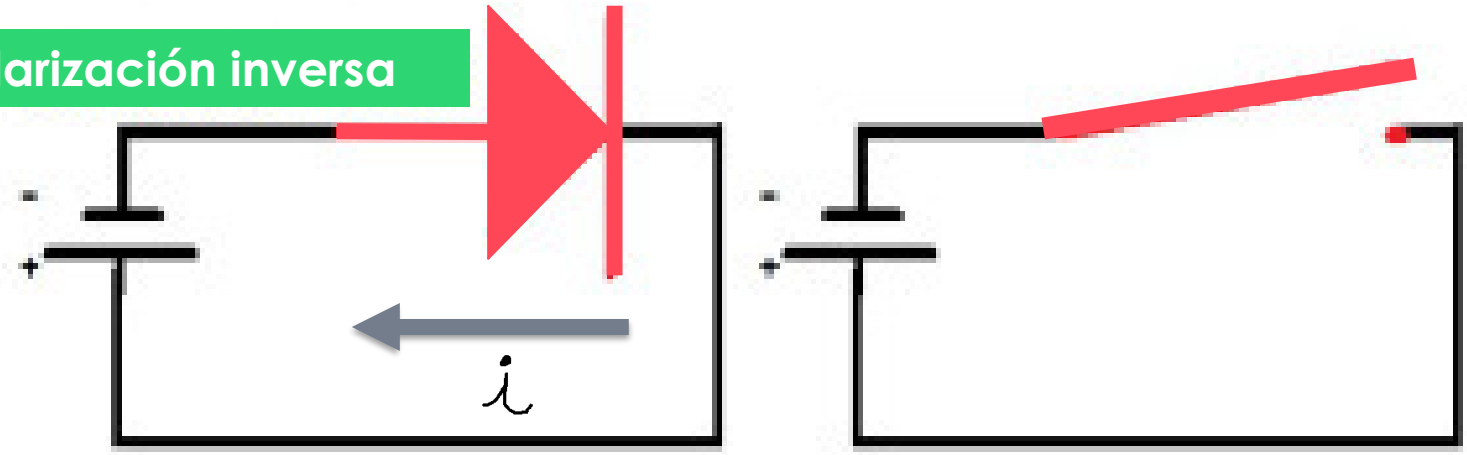
Modelo simplificado lineal (sin avalancha)
Conduce en directa con R=0 a partir de la tensión de la barrera de voltaje , No conduce en inversa



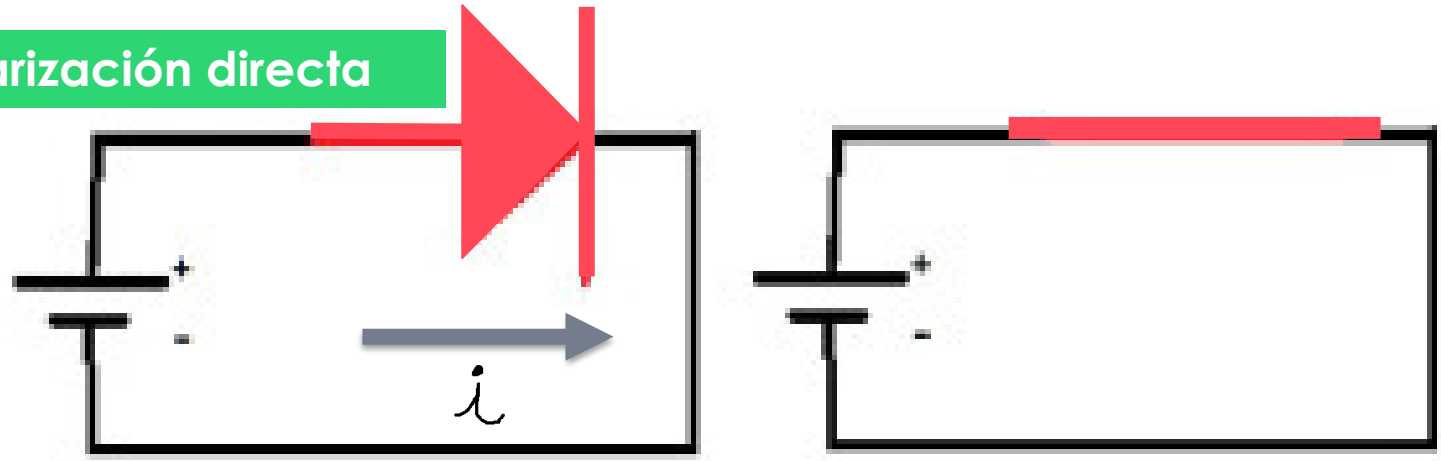


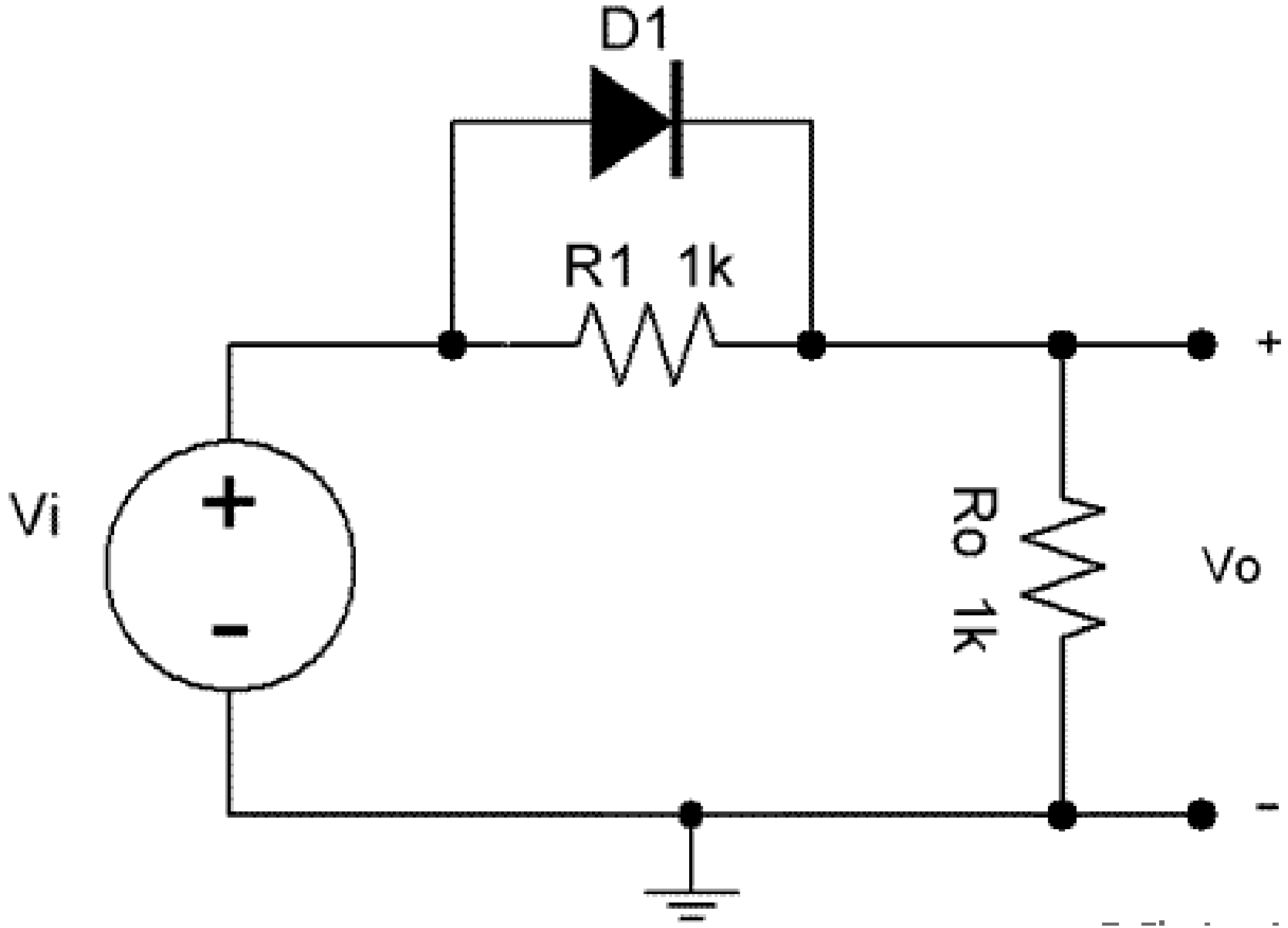
El diodo

Polarización inversa

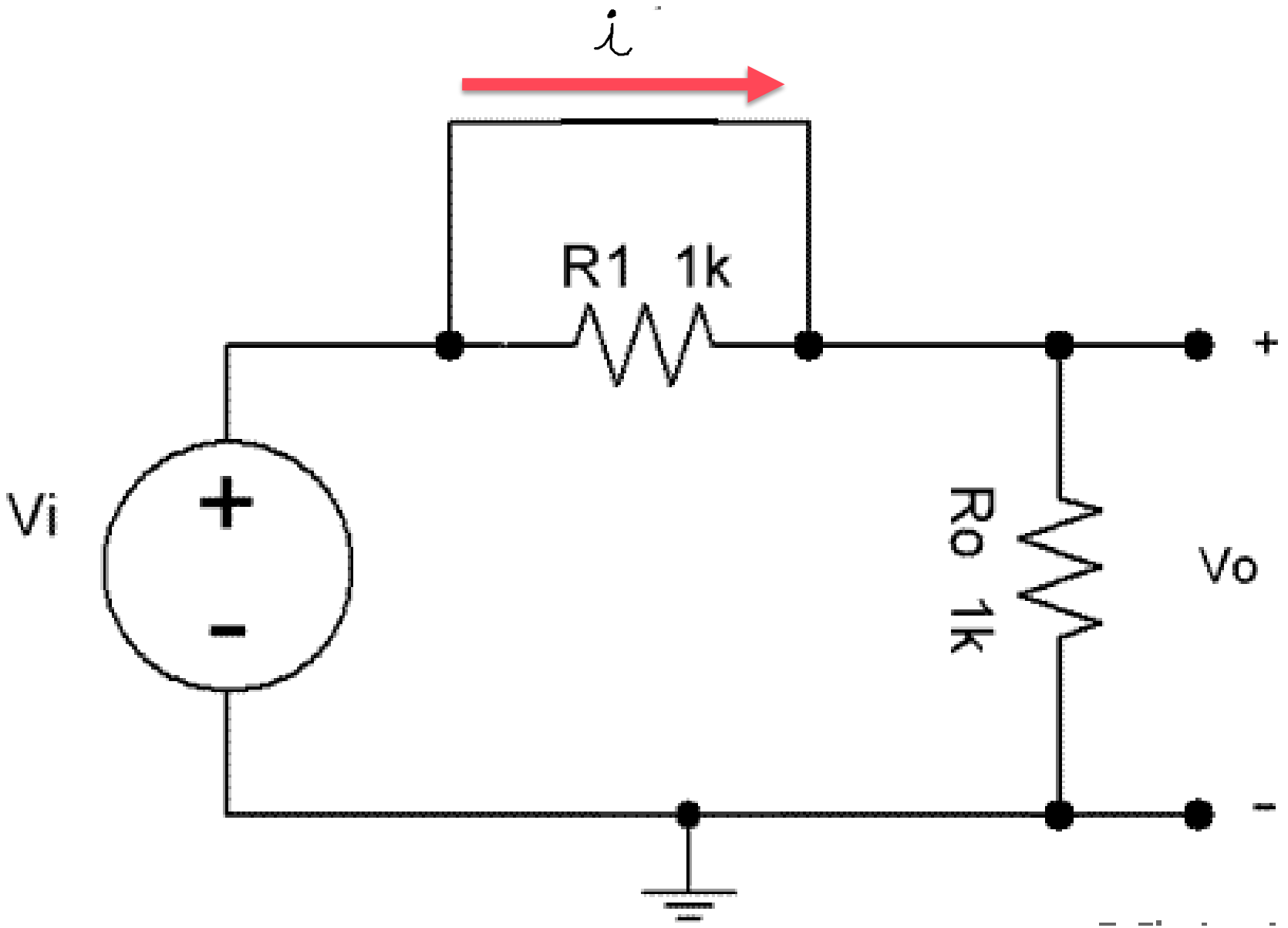


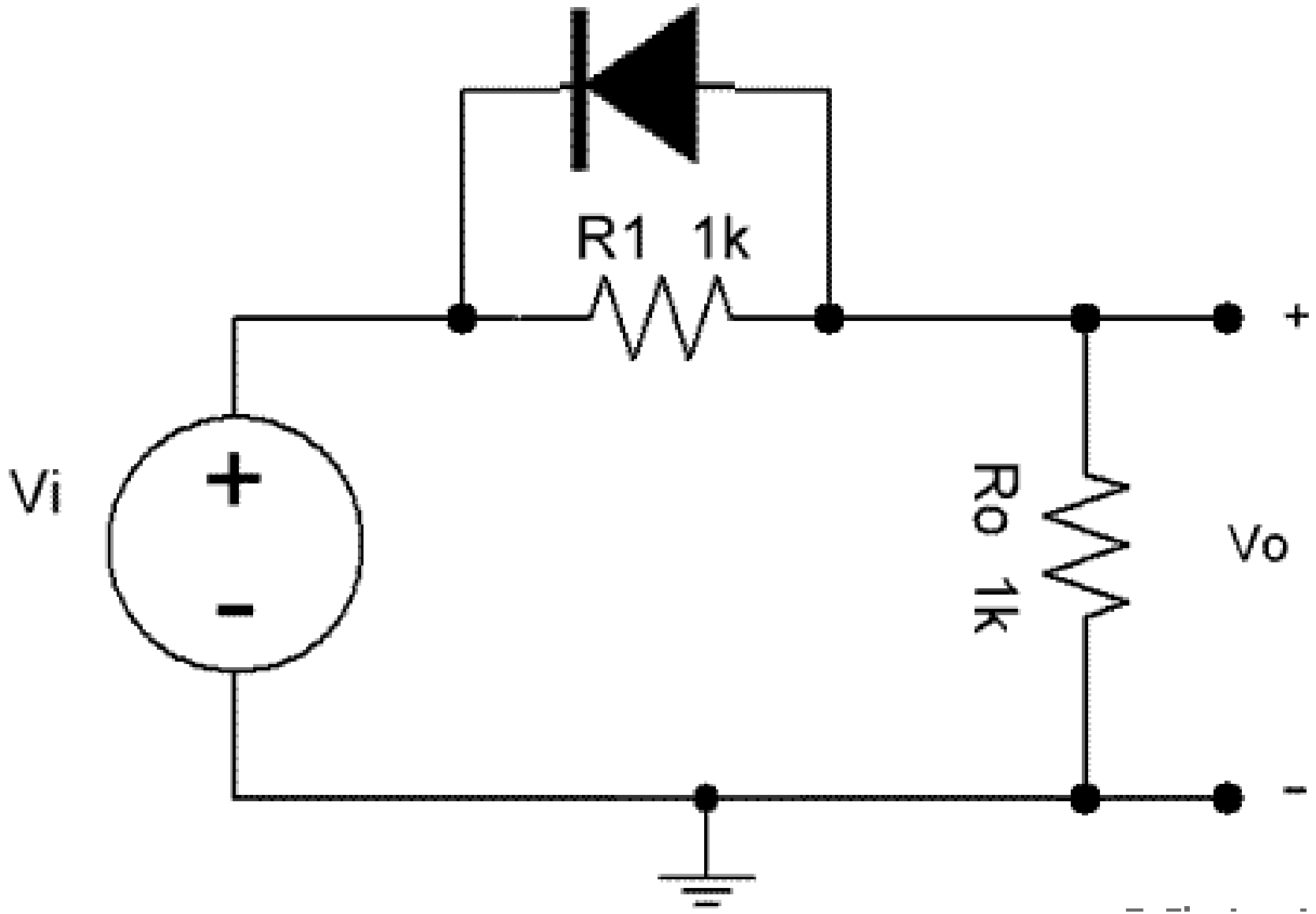
Polarización directa



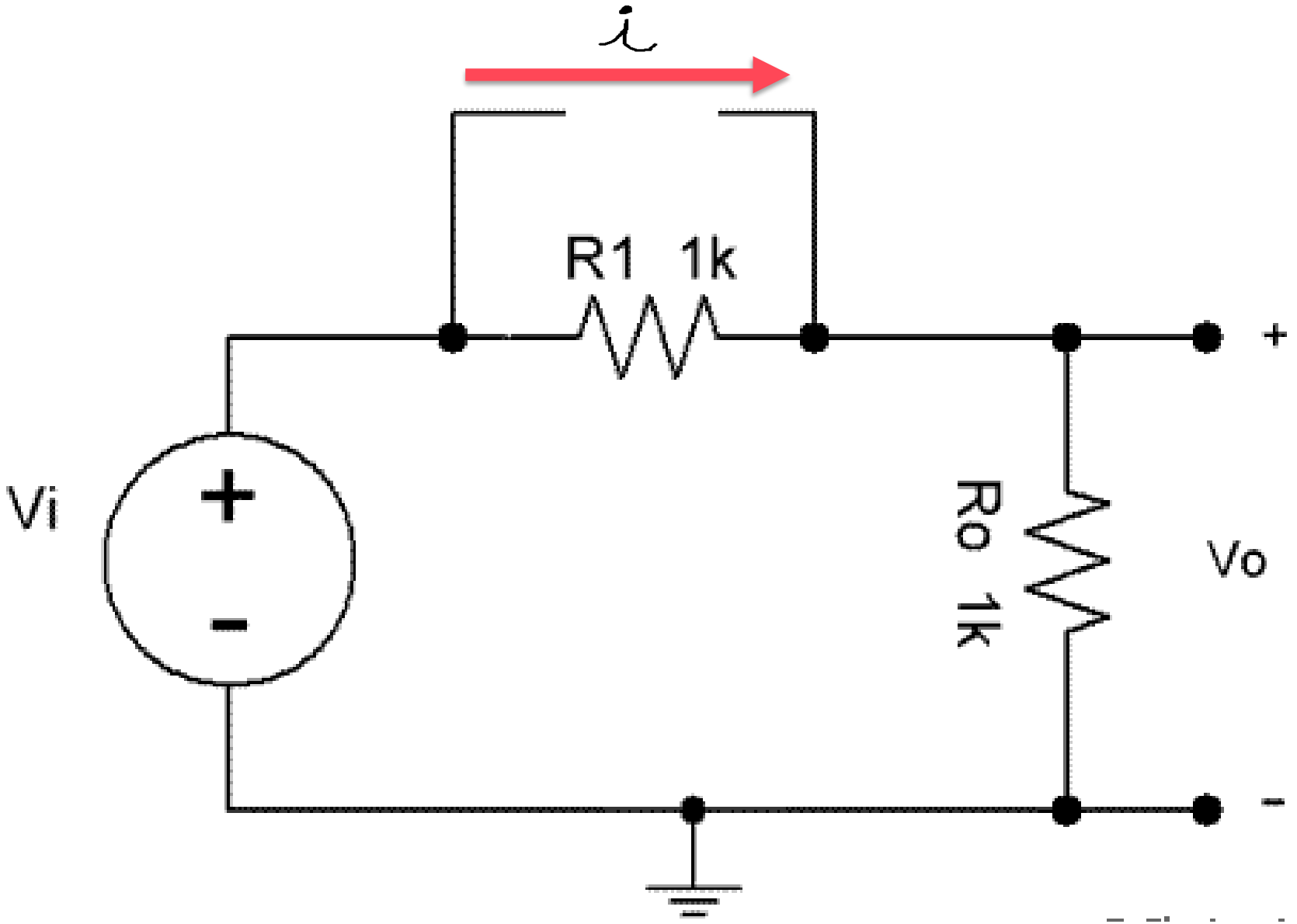

D1
R1 1k
+
Vi
+
-
Ro 1k
Vo
-

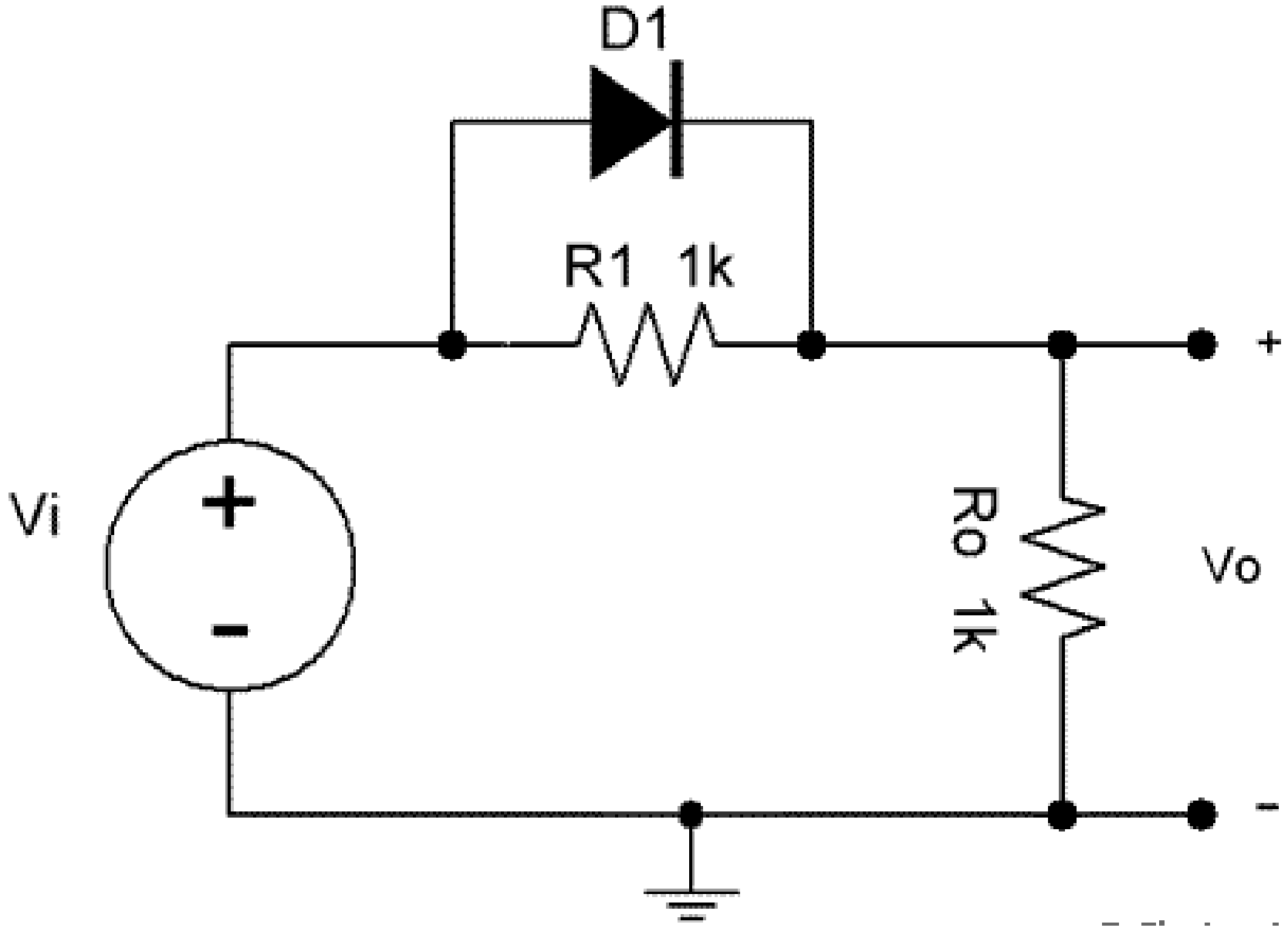
modelo ideal



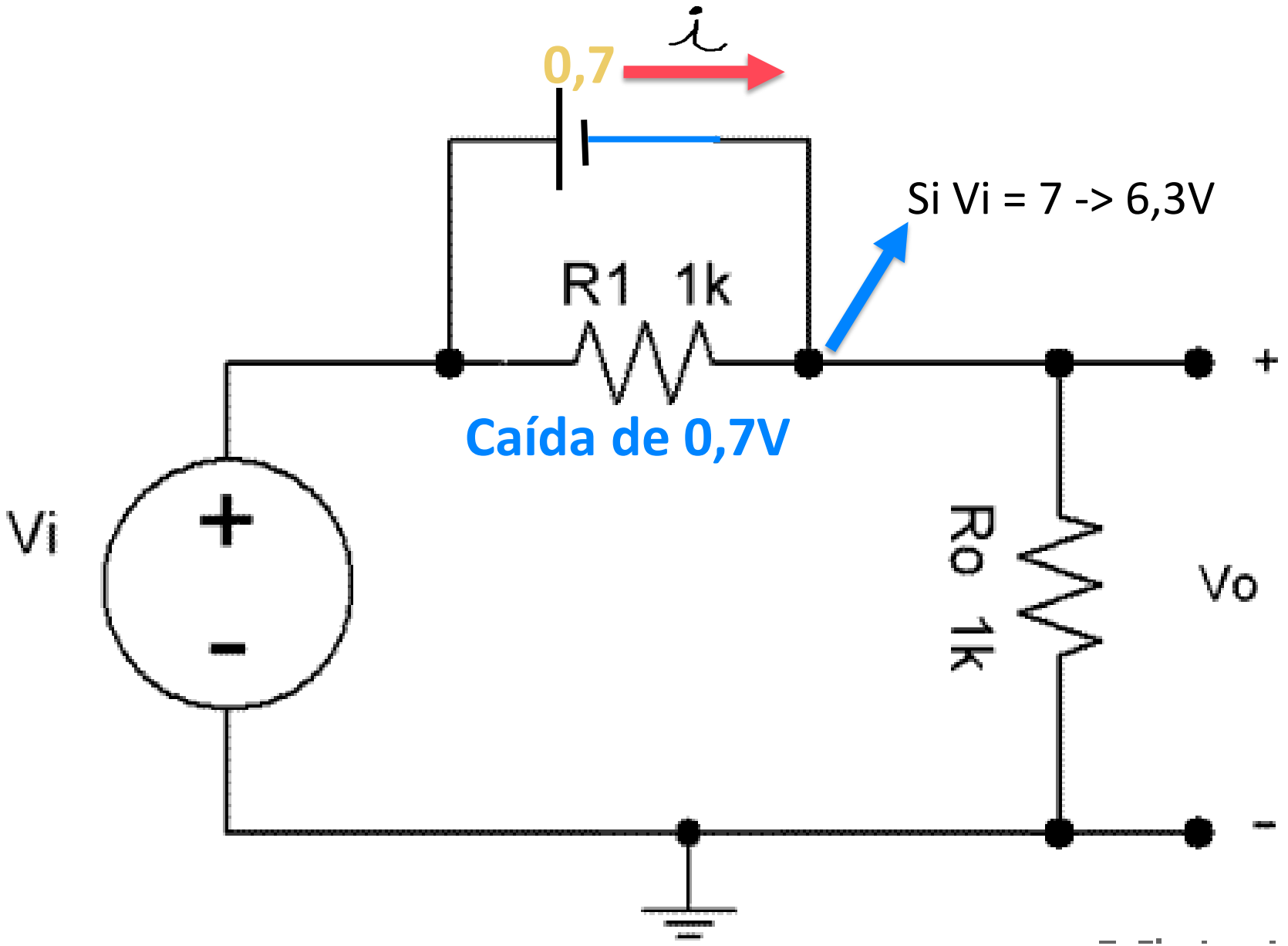

R1 1k
Vi
+
-
Ro 1k
Vo
+
-

modelo ideal

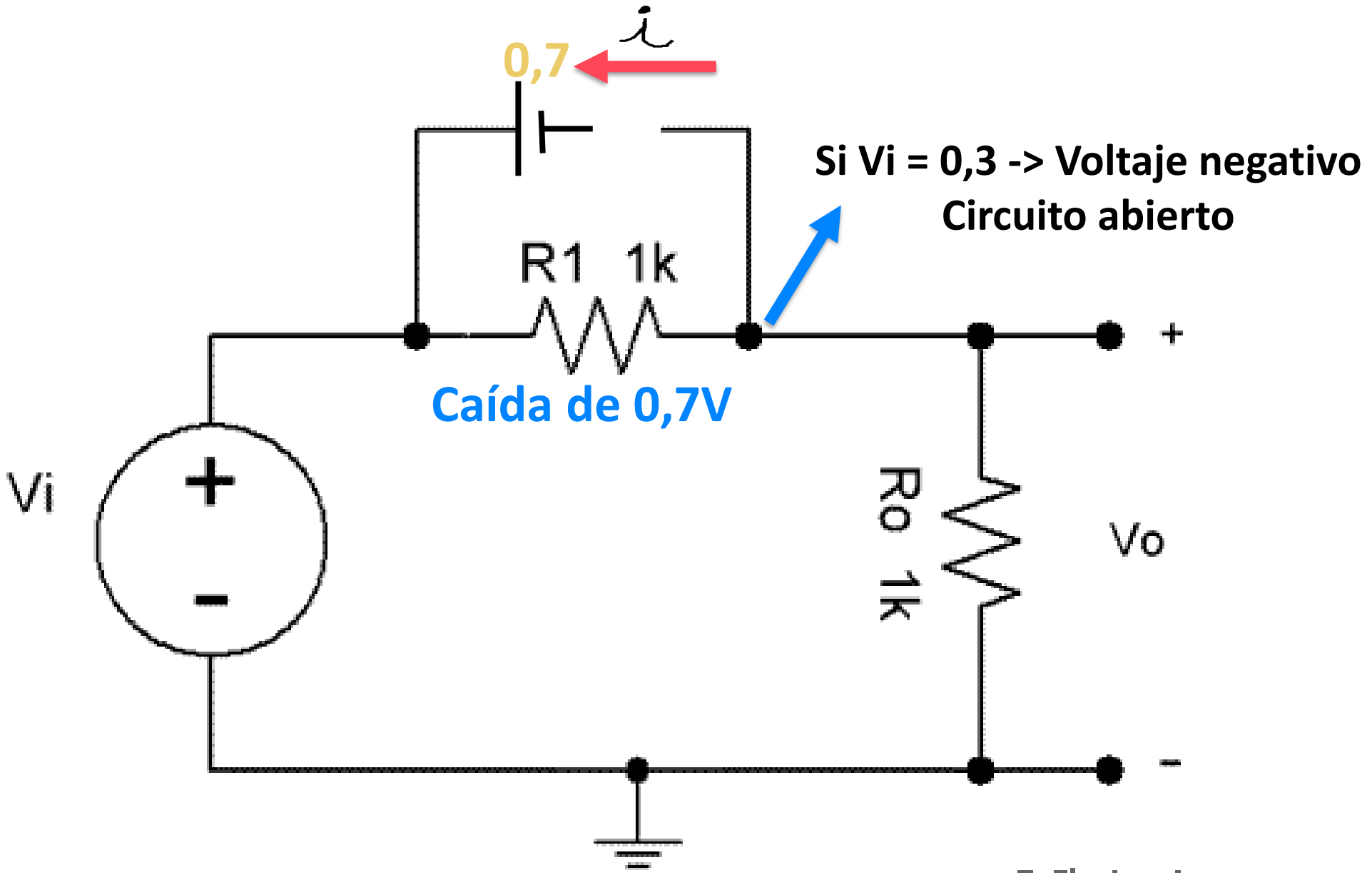



D1
R1 1k
+
Vi
+
-
Ro 1k
Vo
-

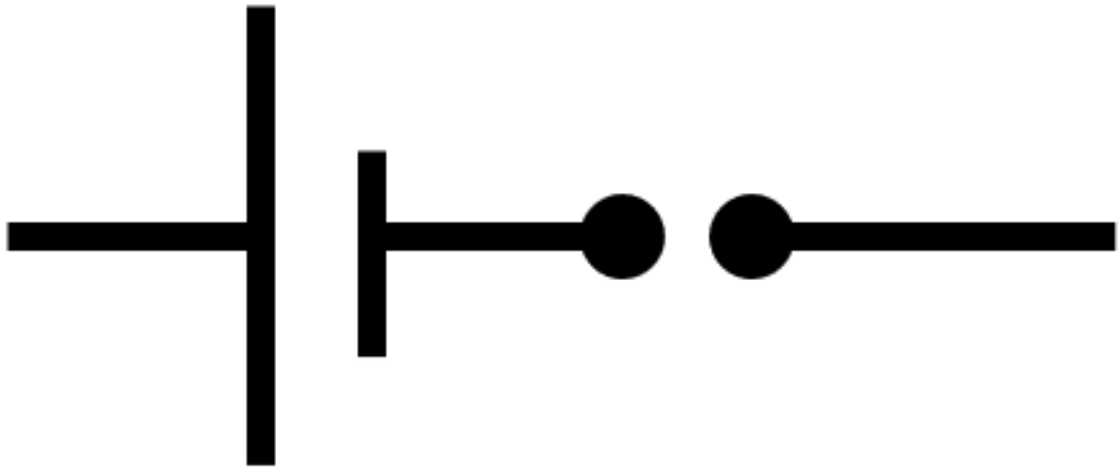
modelo aproximado



modelo aproximado

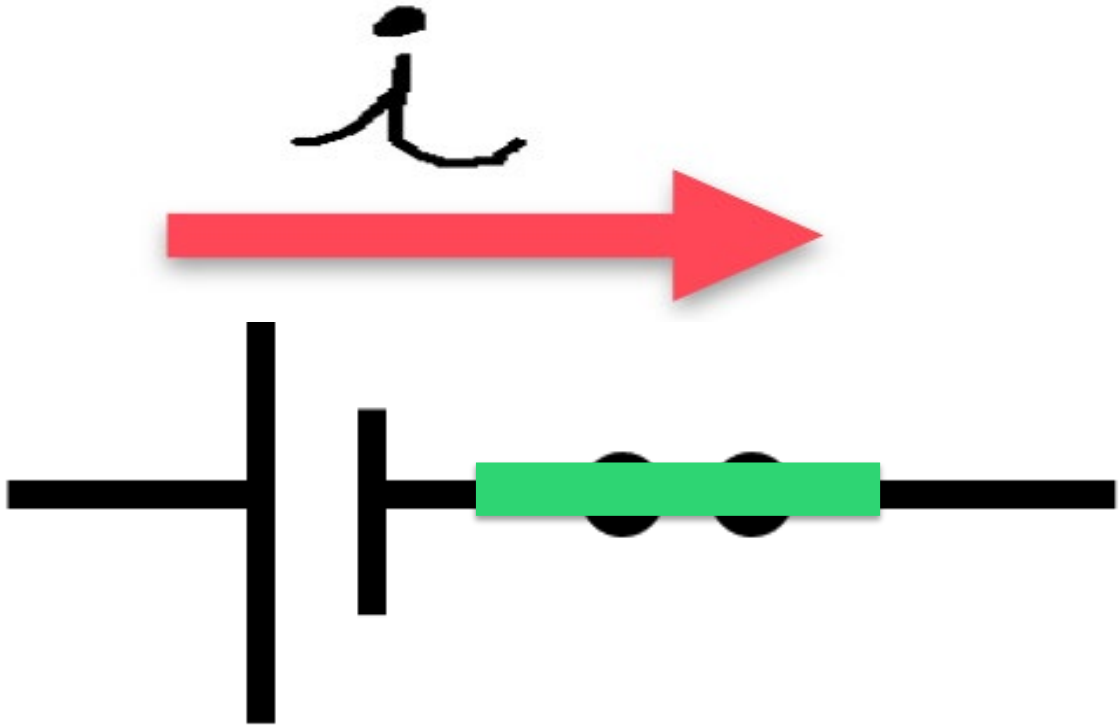


modelo aproximado



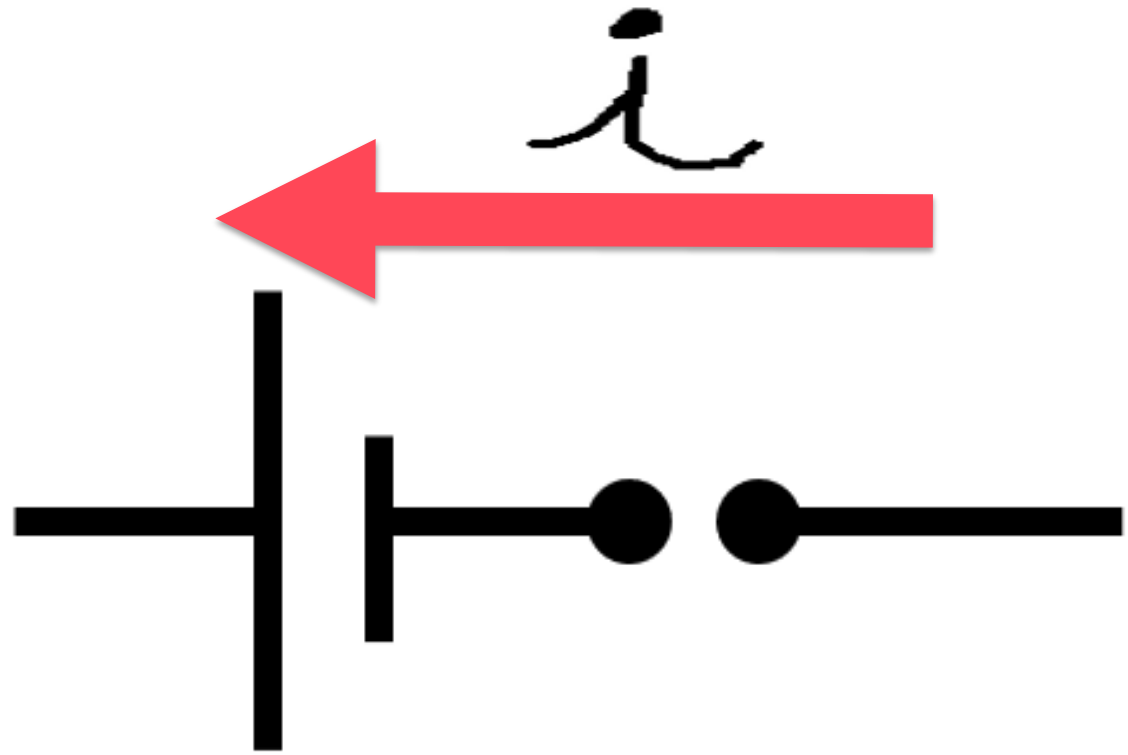
fuente en inversa + modelo ideal

modelo aproximado

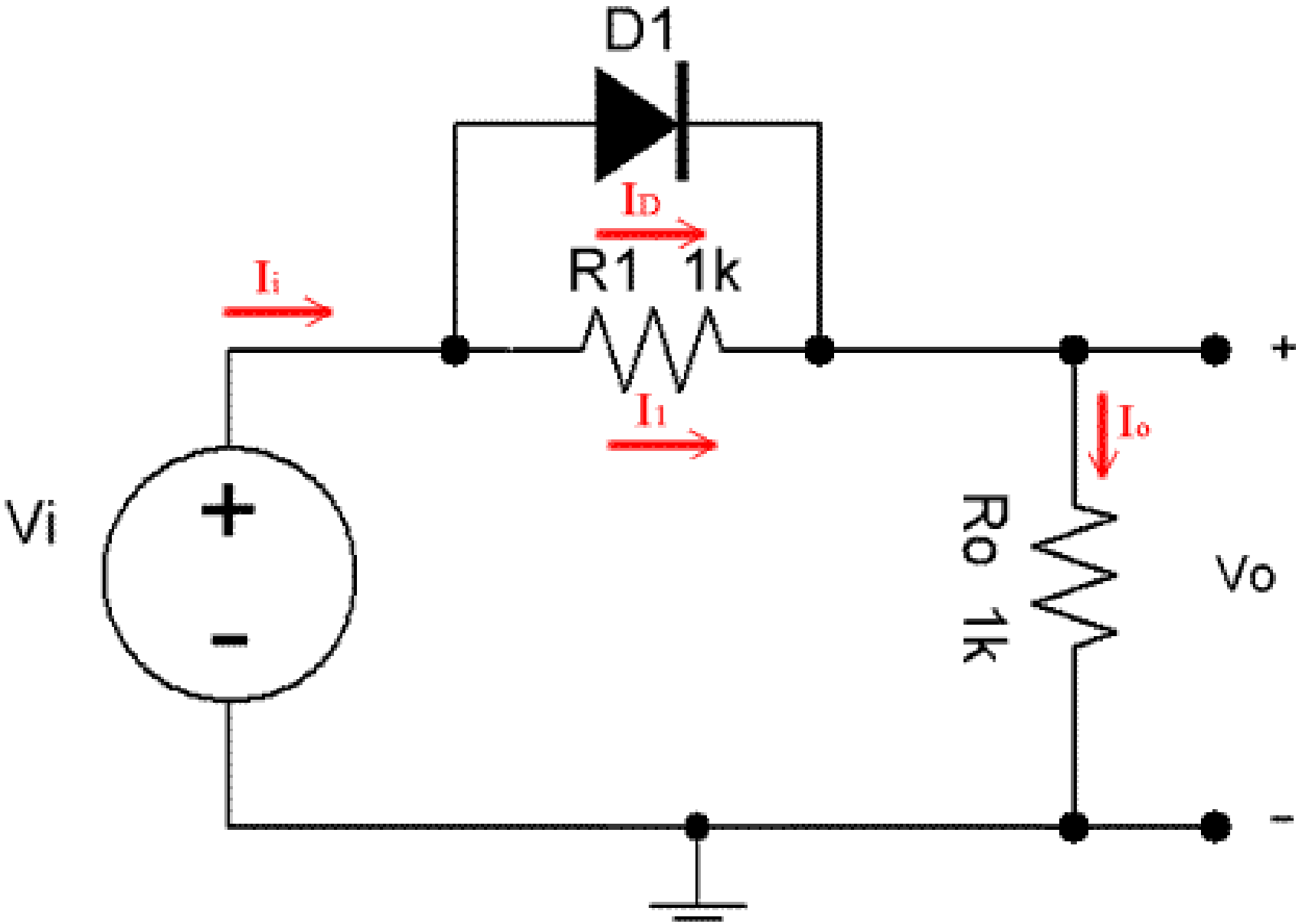


fuente en inversa + modelo ideal

modelo aproximado



fuente en inversa + modelo ideal

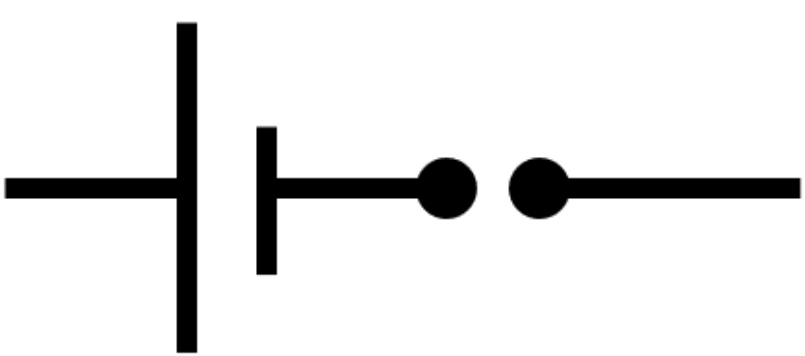

D1
I_D
R1 1k
I_i
I_1
I_o
Vi
+
-
Ro 1k
Vo
+
-

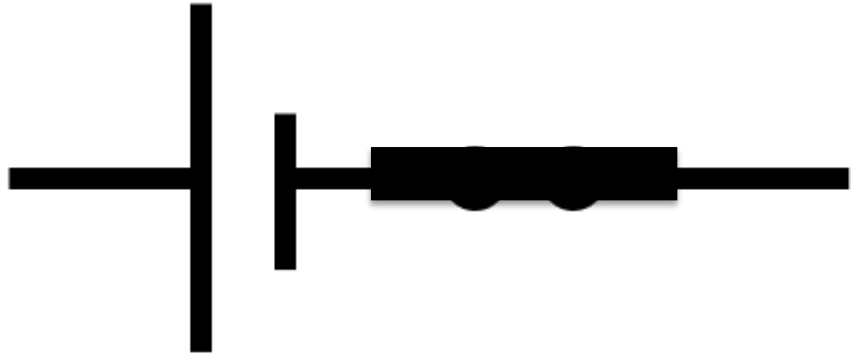
1º Sustituimos el Diodo por su modelo: (ideal)

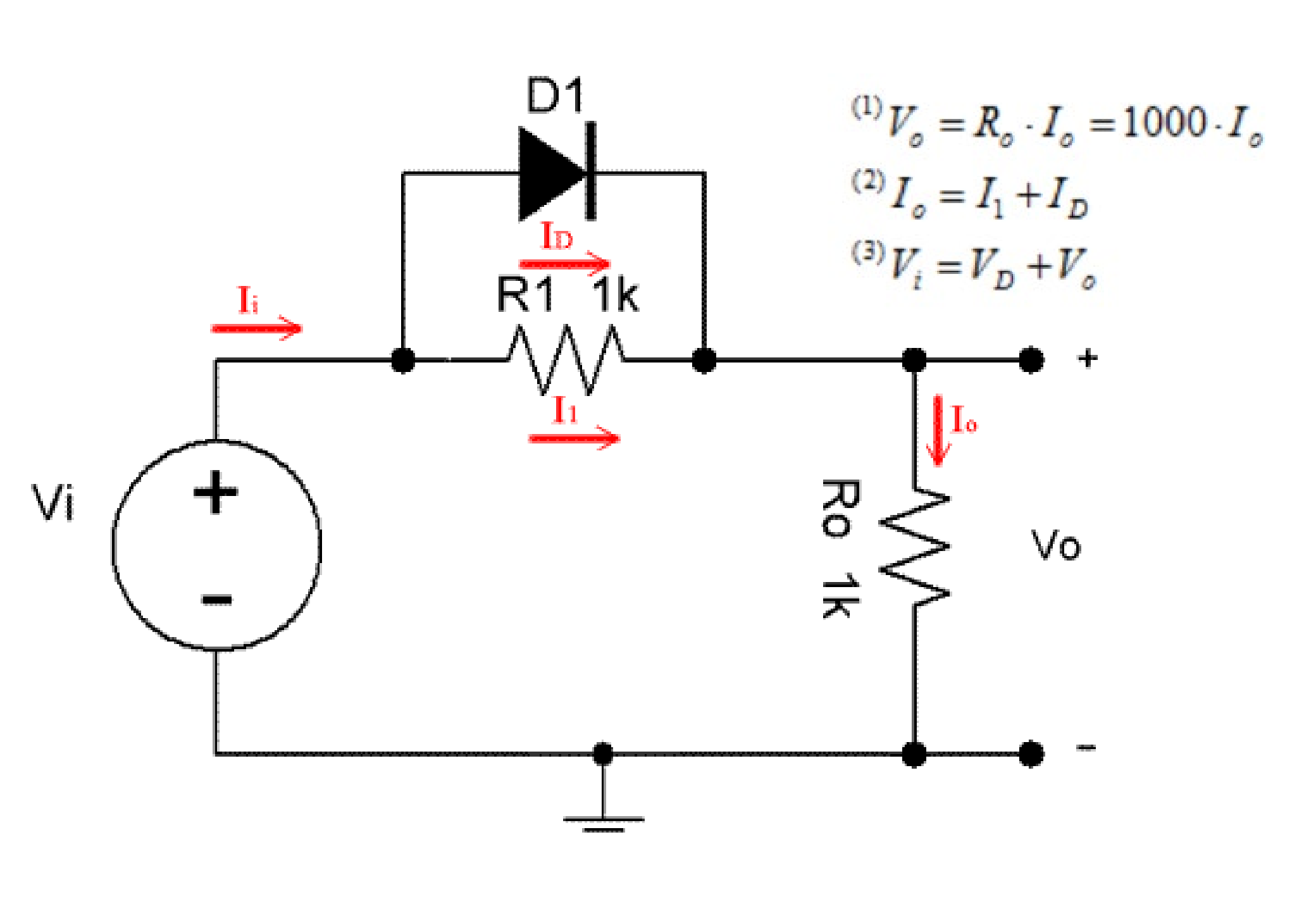
establecemos las intensidades (Kirchhoff)

1º Sustituimos el Diodo por su modelo: (aproximado)

establecemos las intensidades (Kirchhoff)







$$(1)\ V_o = R_o \cdot I_o = 1000 \cdot I_o$$

$$(2)\ I_o = I_1 + I_D$$

$$(3)\ V_i = V_D + V_o$$

Caso 1 (modelo aproximado)

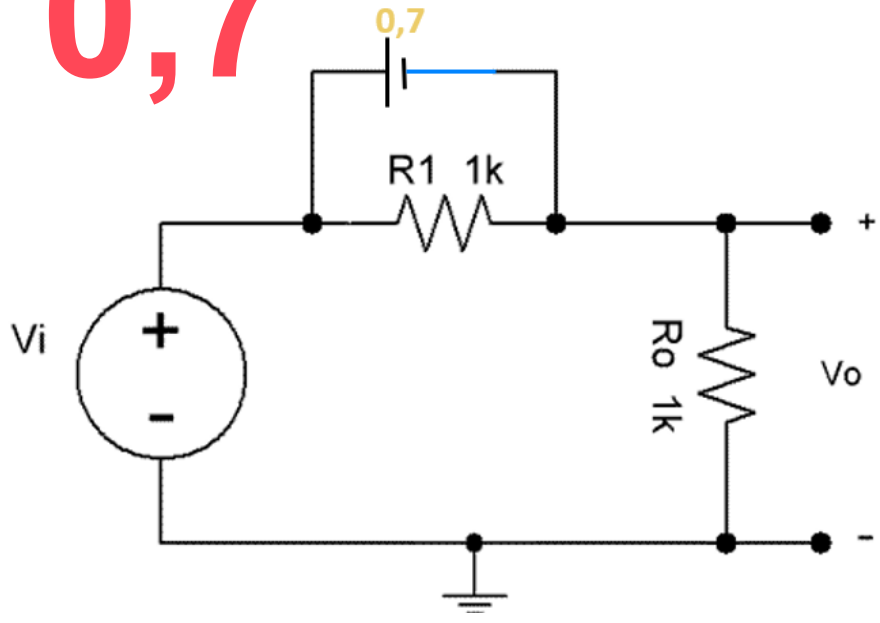
Supongamos que el diodo conduce (establecemos así **i**)

Entonces: $V_D = 0{,}7V = V_\gamma$

$$\mathbf{V_o = V_i - 0{,}7}$$

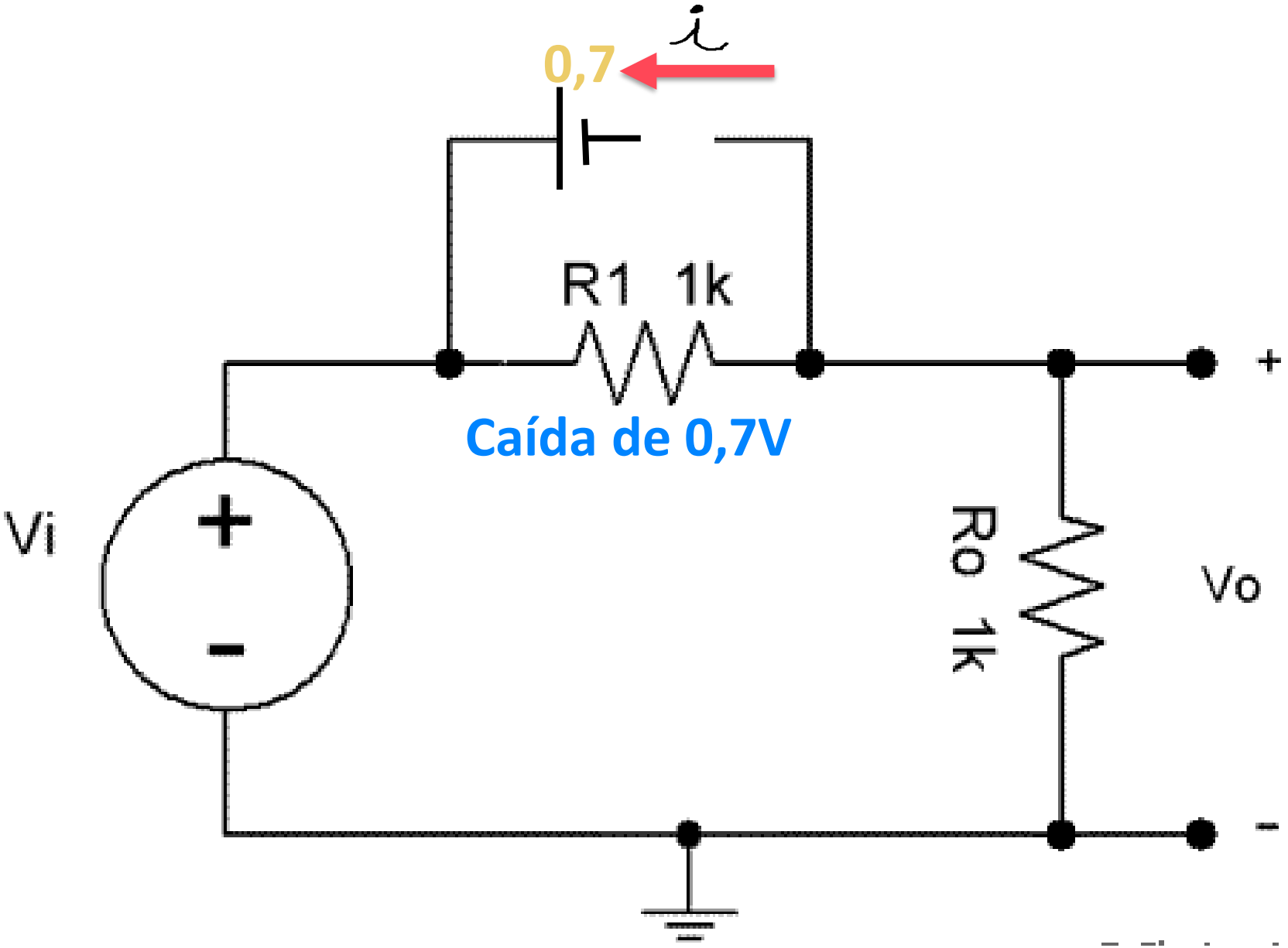
$$I_1 = \frac{V_D}{R_1} = \frac{0{,}7}{1000} = 0{,}7 \cdot 10^{-3} A$$

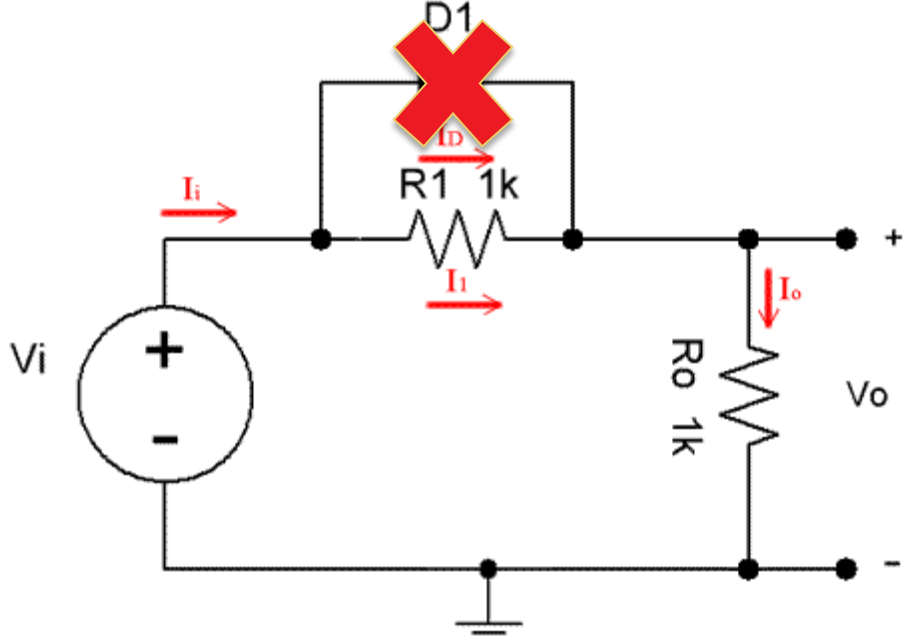
$$I_o = \frac{V_o}{R_o} = \frac{V_i - 0{,}7}{1000}$$



Caso 2 (modelo aproximado)

El diodo NO conduce.

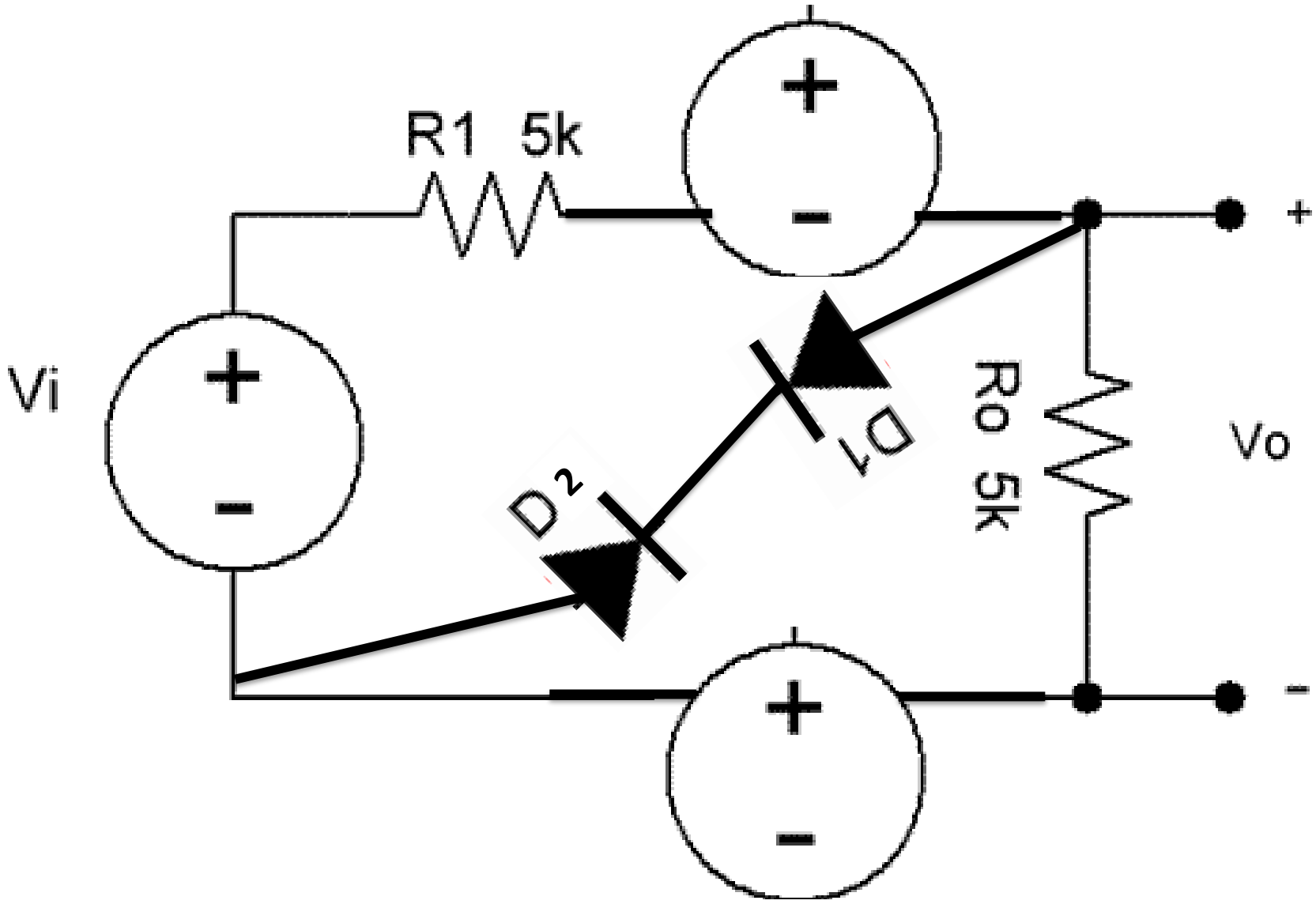




Entonces: $I_D = 0$

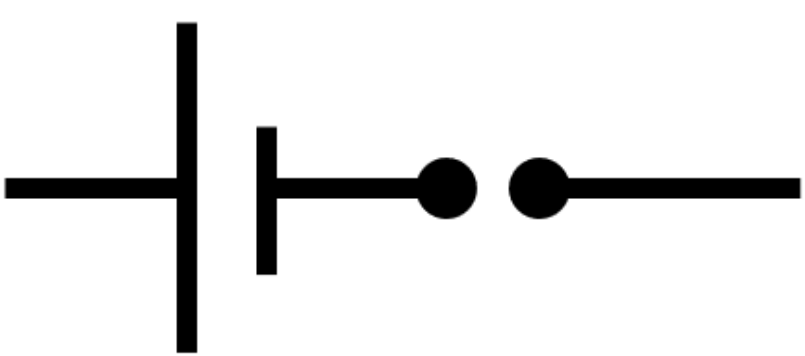
$$(2)\ I_o = I_1 + I_D = I_1$$

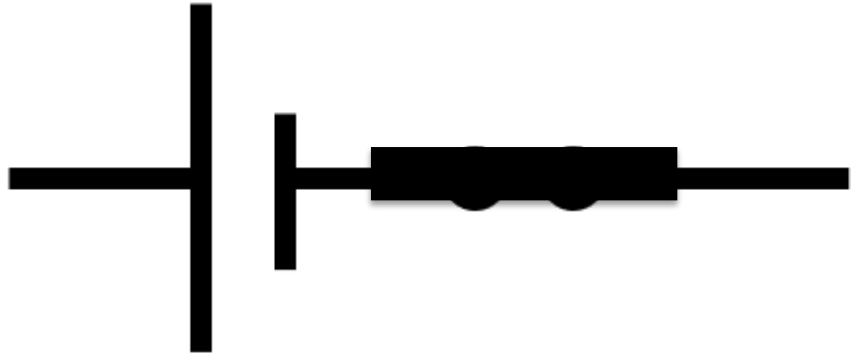
$$(3)\ V_i = V_D + V_o = R_1 \cdot I_1 + R_o \cdot I_o$$

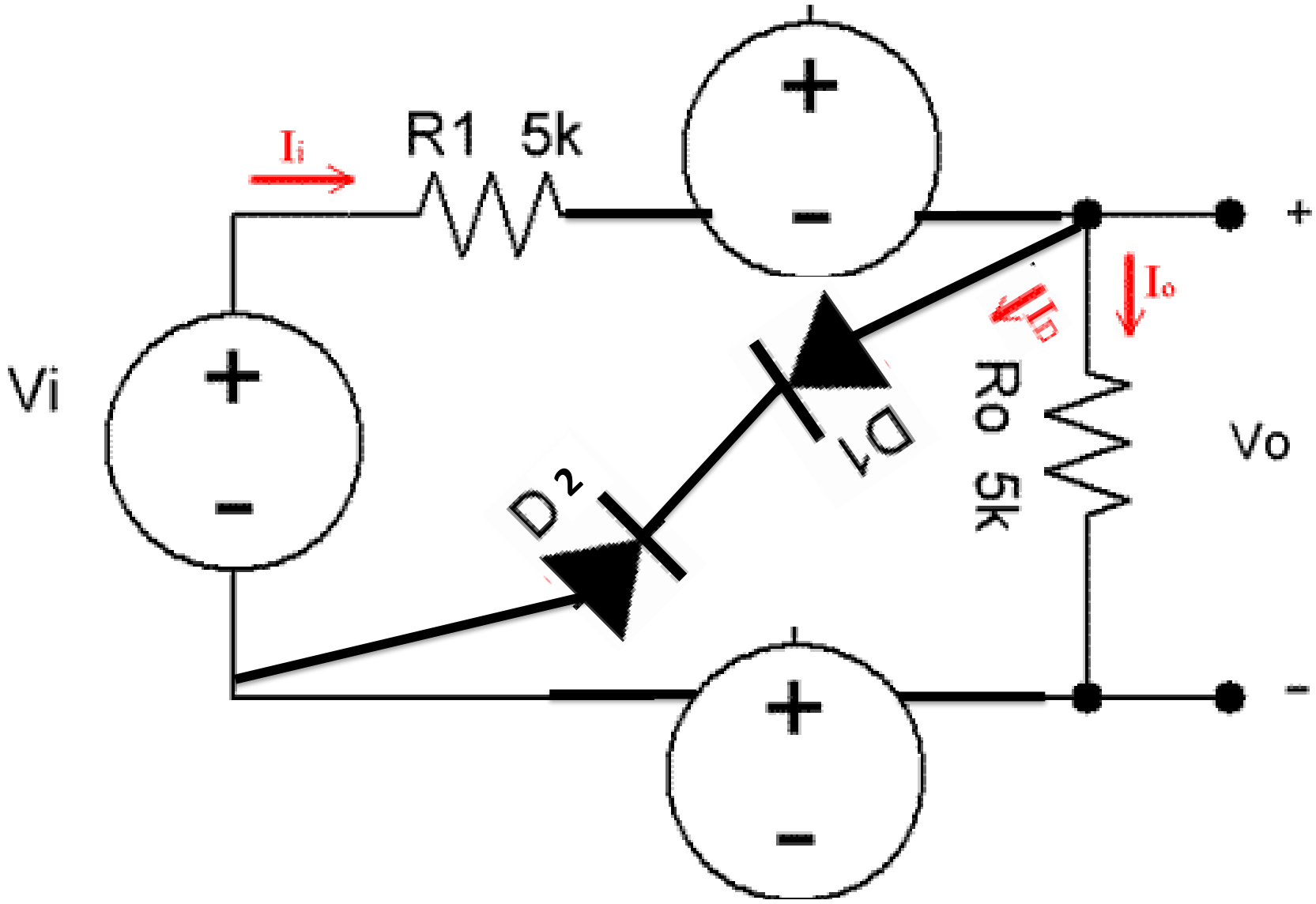

R1 5k
Vi
D2
D1
Ro 5k
Vo
+
-

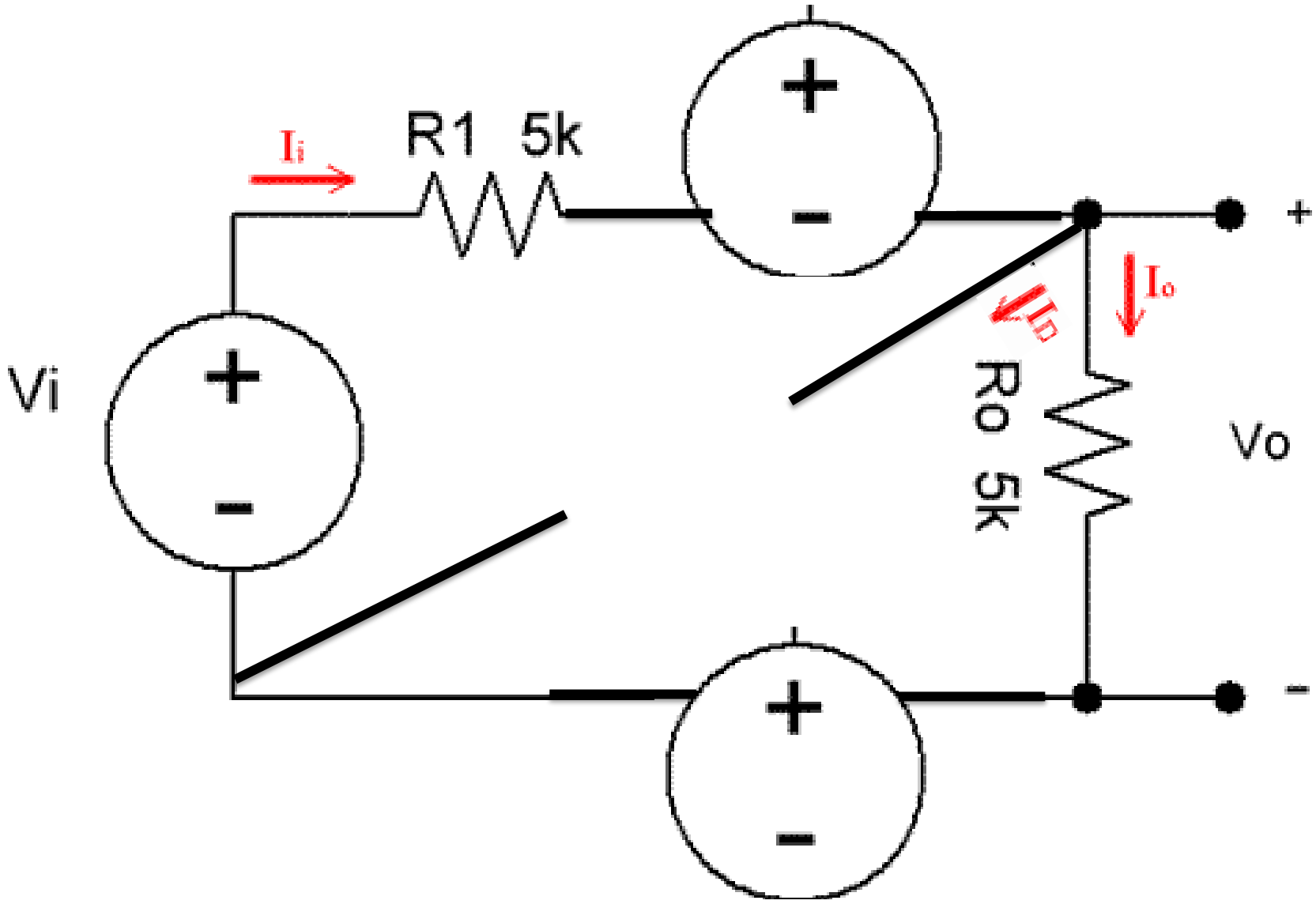
1º Sustituimos el Diodo por su modelo: (aproximado)

establecemos las intensidades (Kirchhoff)



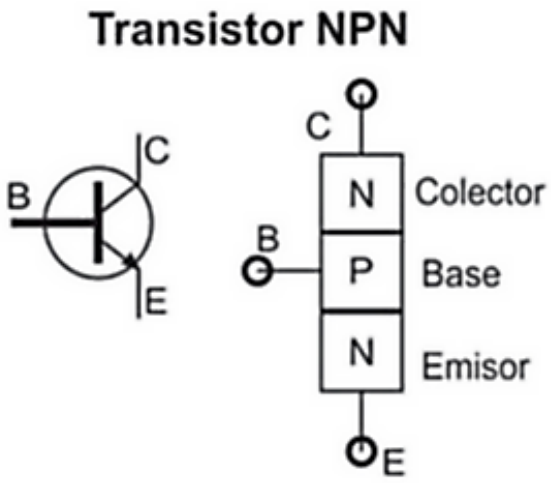


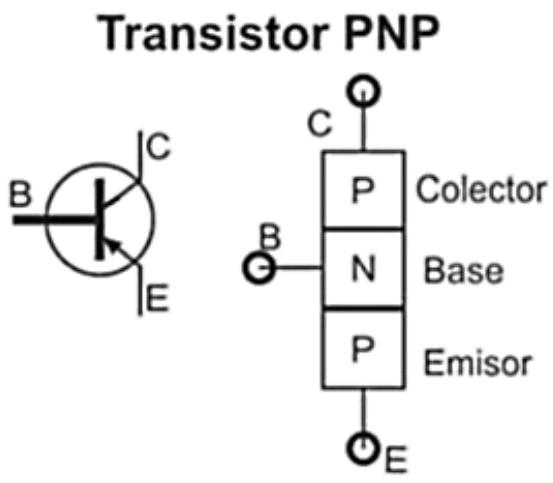

Ii
R1 5k
Vi
D2
D1
ID
Io
Ro 5k
Vo
+
-

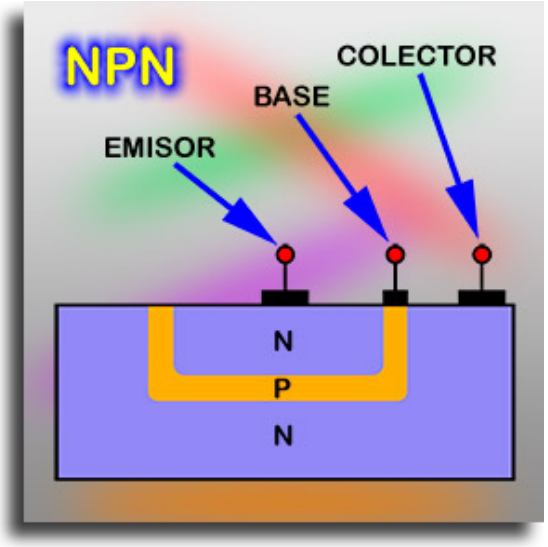

Ii
R1 5k
Vi
Io
Ro 5k
Vo
+
-

Transistor BJT (Bipolar)

- NPN o PNP dependiendo de su configuración de uniones
  - Base
  - Colector
  - Emisor





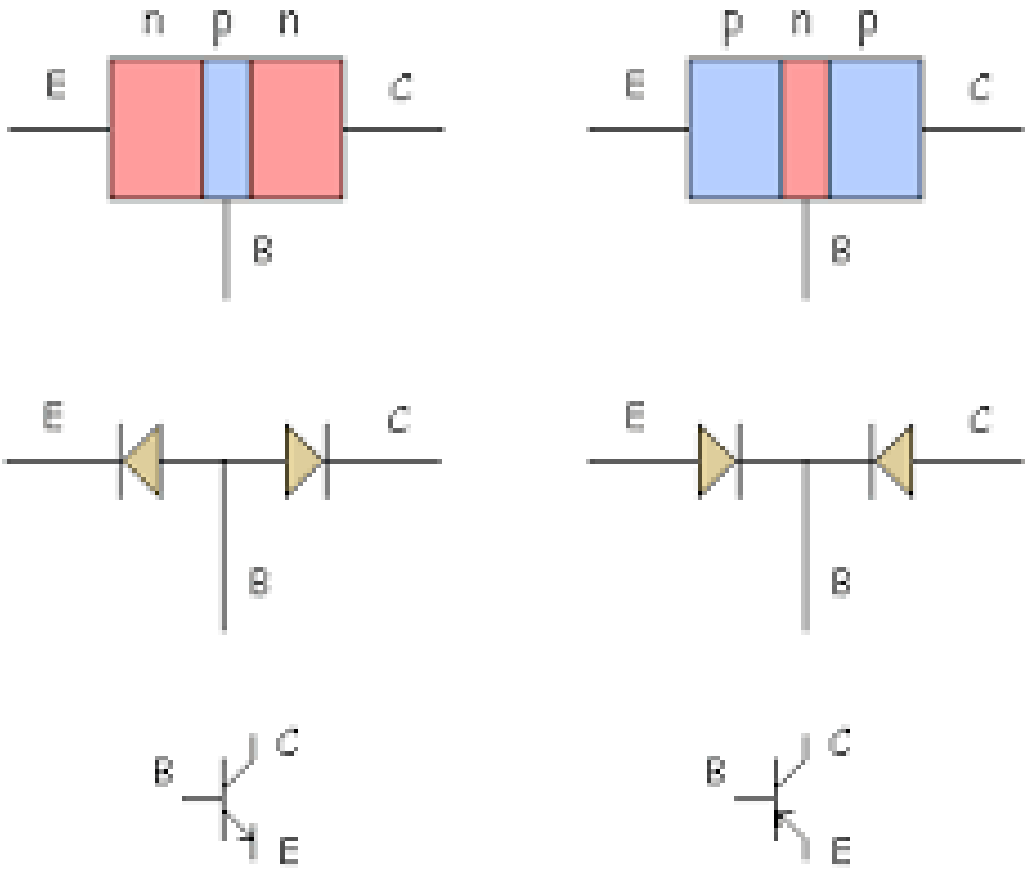


$$\beta = \frac{I_C}{I_B}$$

ß es constante para el transistor (a igual temperatura)

$$I_E = I_C + I_B$$

Transistor BJT (Bipolar)

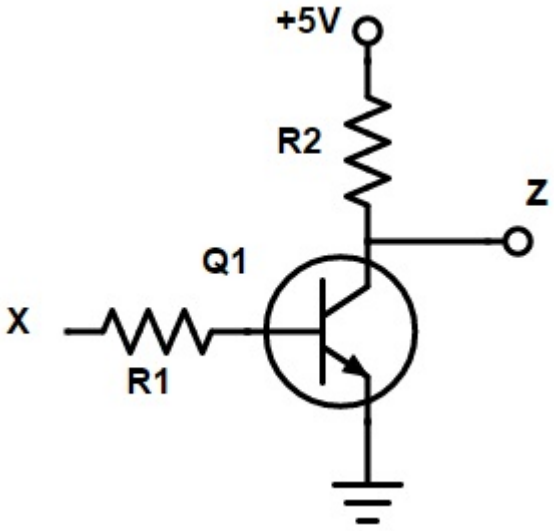


Transistor BJT (Bipolar)

Pueden funcionar como:

interruptores

amplificadores



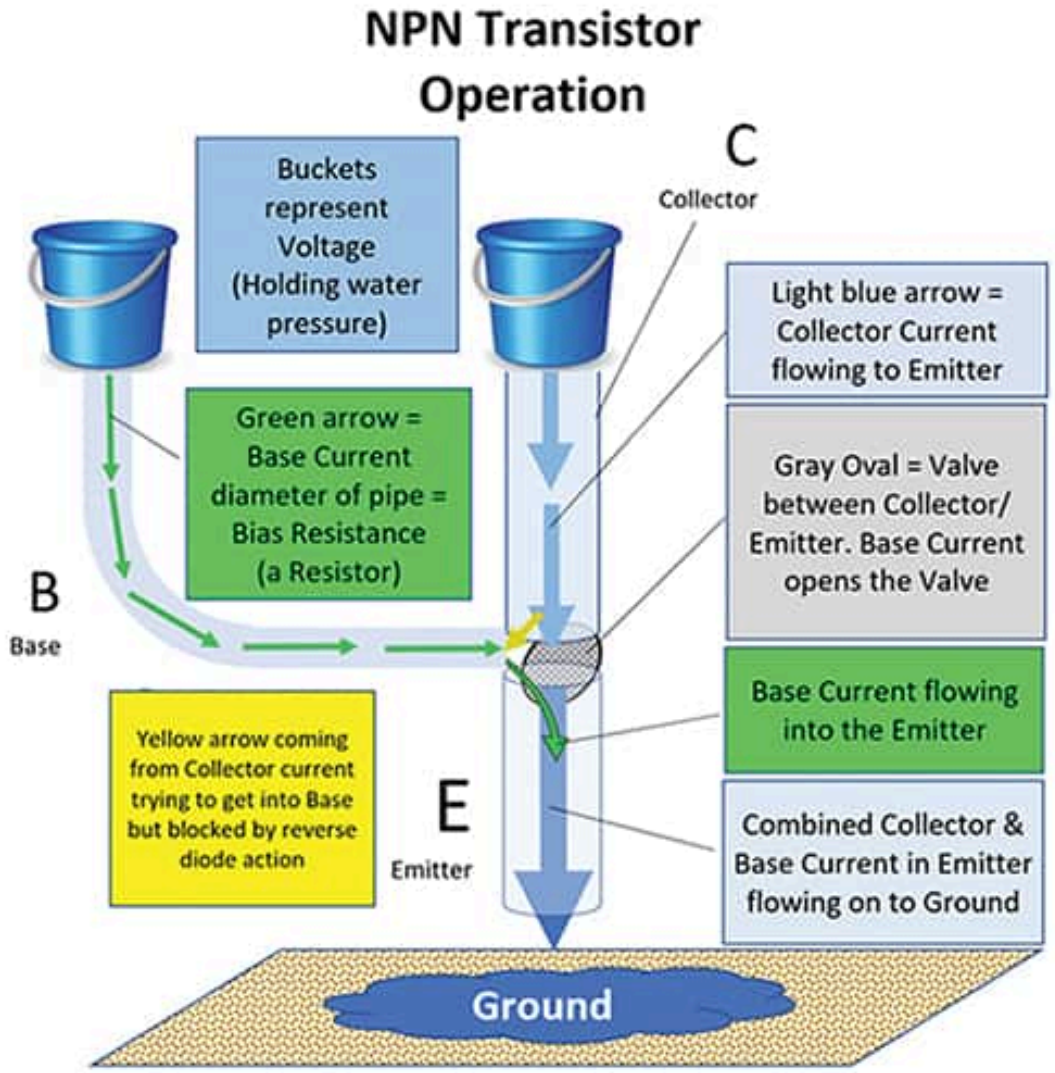
$$\beta = \frac{I_C}{I_B}$$

$$I_E = I_C + I_B$$

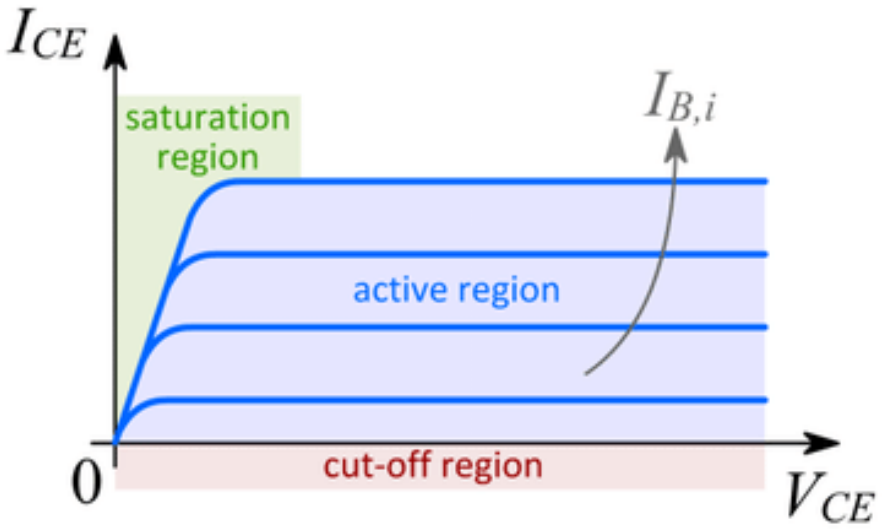
1 - deja pasar, se convierte en un CLABLE

O - no deja pasar

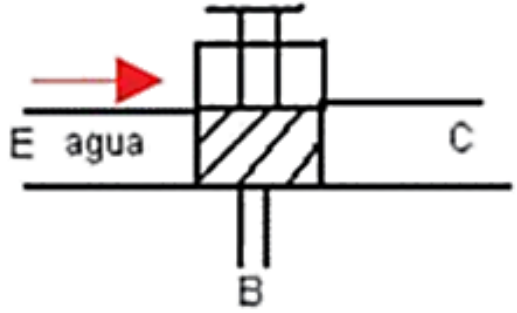
BJT


NPN Transistor Operation
Buckets represent Voltage (Holding water pressure)
C
Collector
Light blue arrow = Collector Current flowing to Emitter
Green arrow = Base Current diameter of pipe = Bias Resistance (a Resistor)
Gray Oval = Valve between Collector/ Emitter. Base Current opens the Valve
B
Base
Base Current flowing into the Emitter
Yellow arrow coming from Collector current trying to get into Base but blocked by reverse diode action
E
Emitter
Combined Collector & Base Current in Emitter flowing on to Ground
Ground

BJT : Regiones activa, corte y saturación

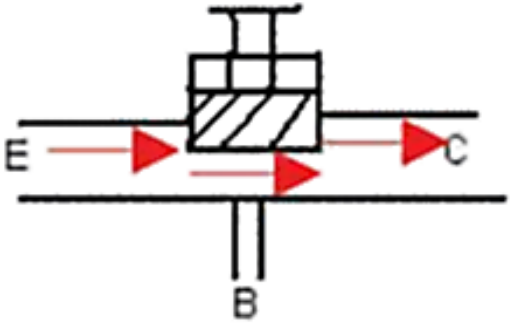


En corte: no deja pasar el agua "corriente" (corriente cero).



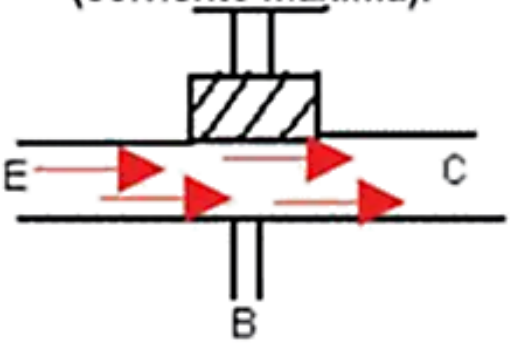
En Corte

En activa : deja pasar más agua "corriente" (corriente variable).



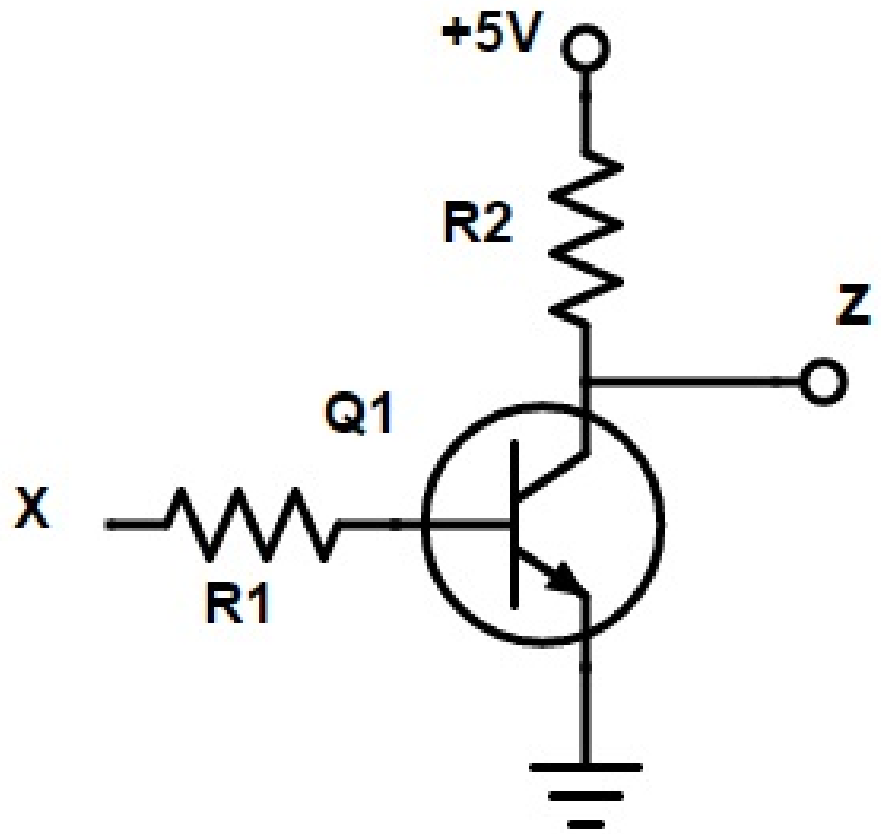
En activa

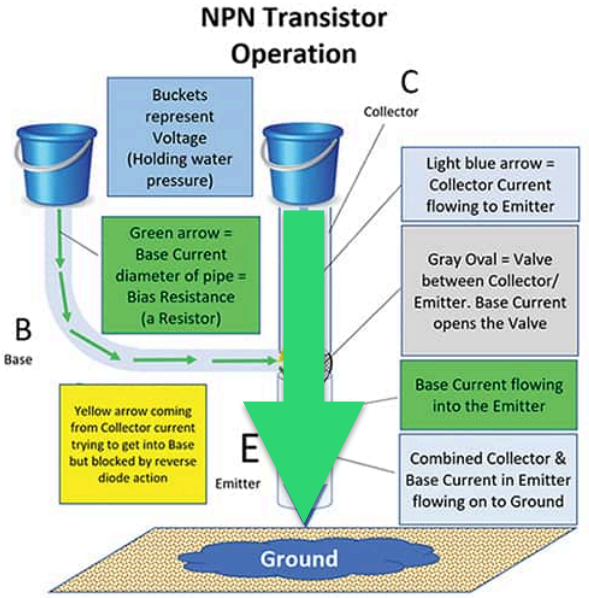
En saturación: deja pasar toda la agua "corriente" (corriente máxima).



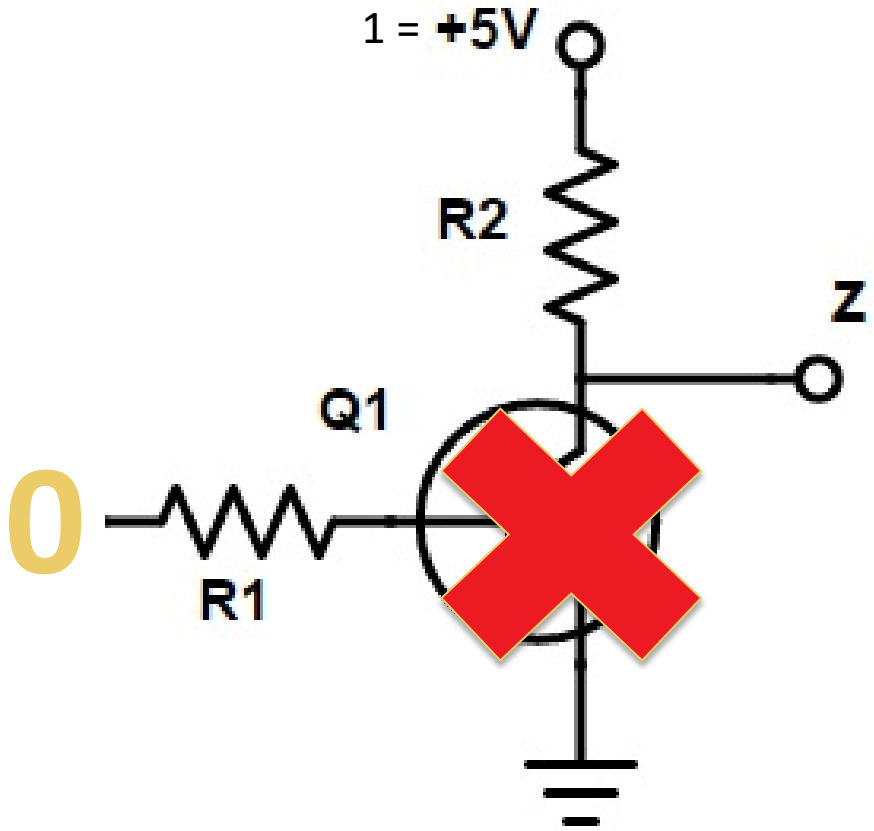
En Saturación

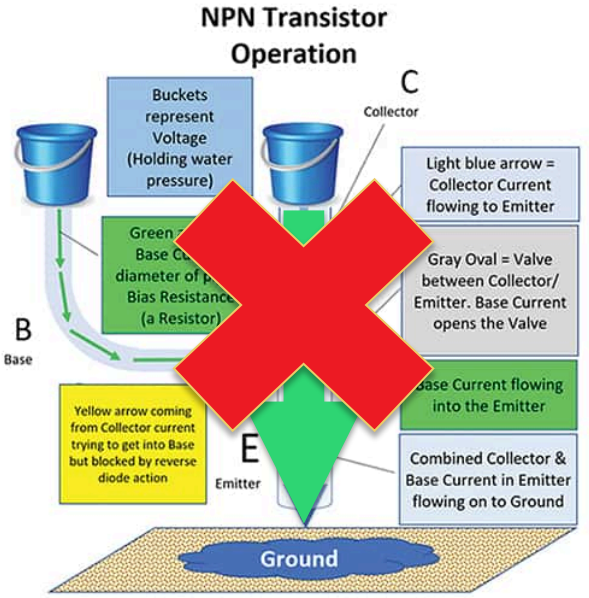
Puerta NOT con NPN



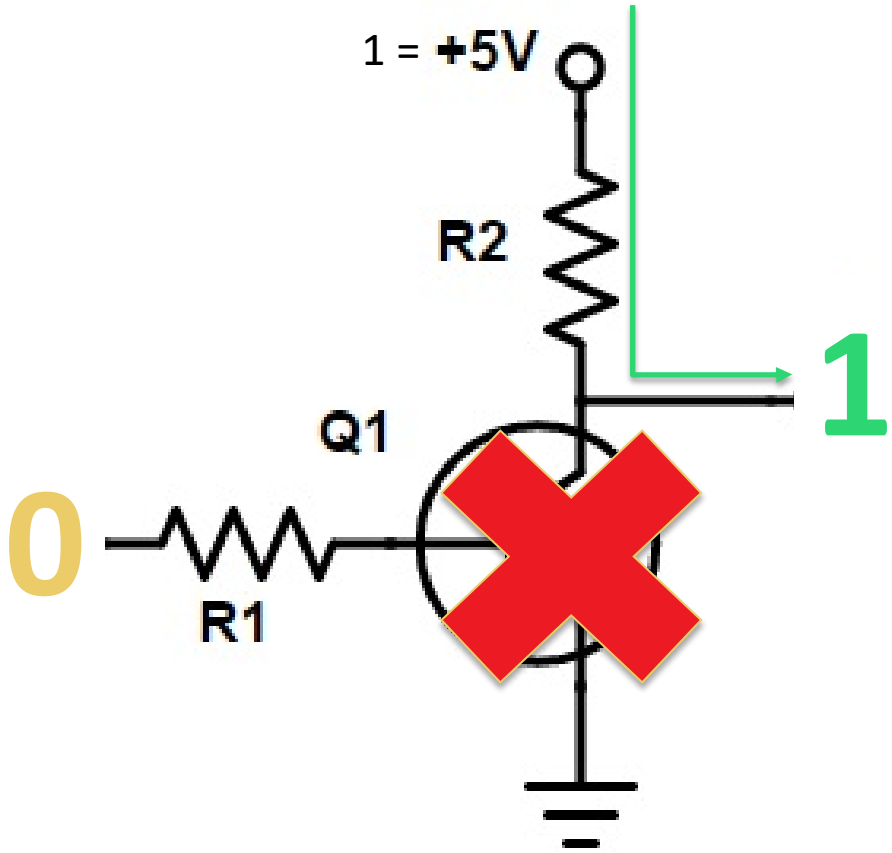


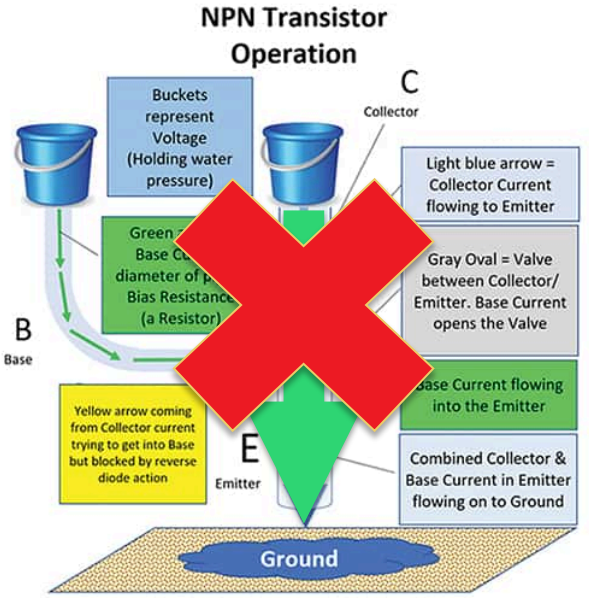
Puerta NOT con NPN



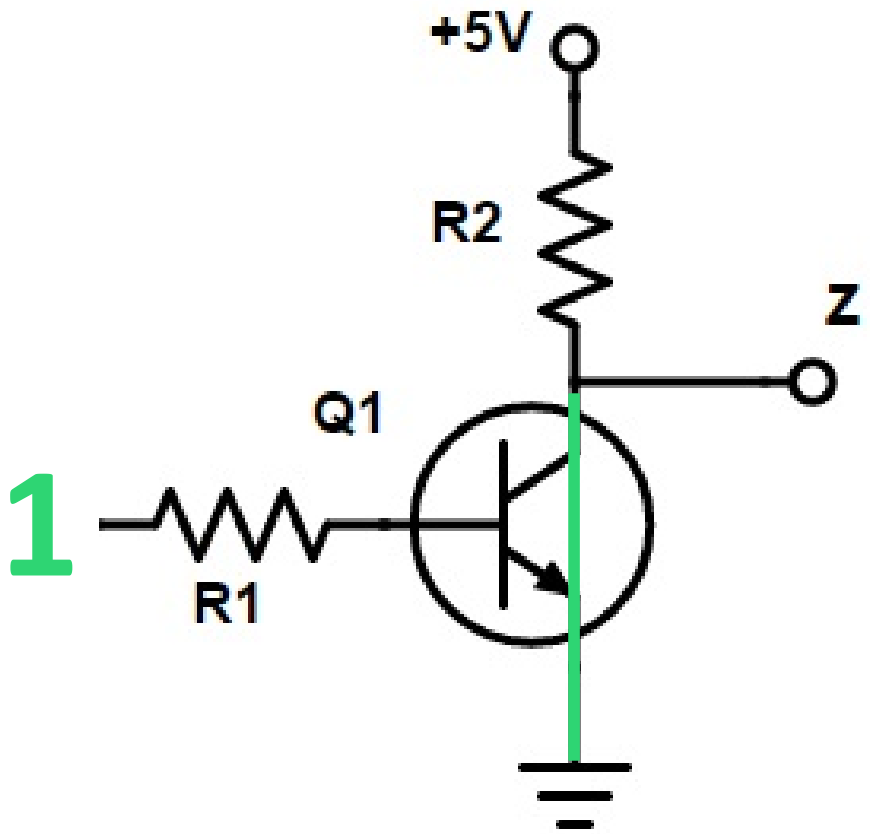


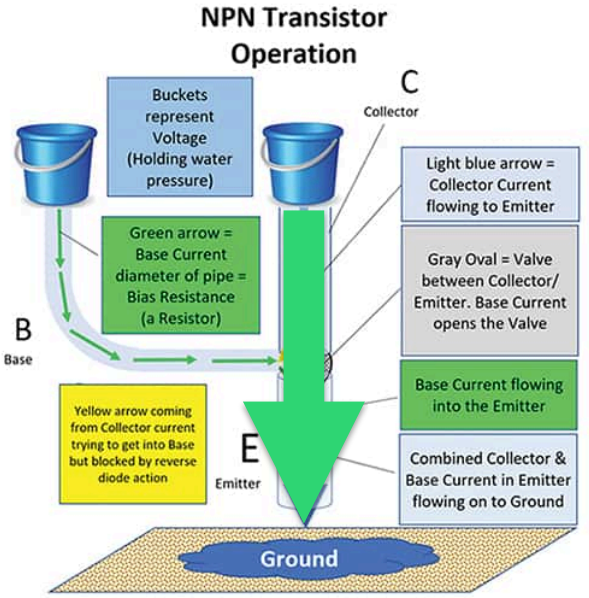
Puerta NOT con NPN



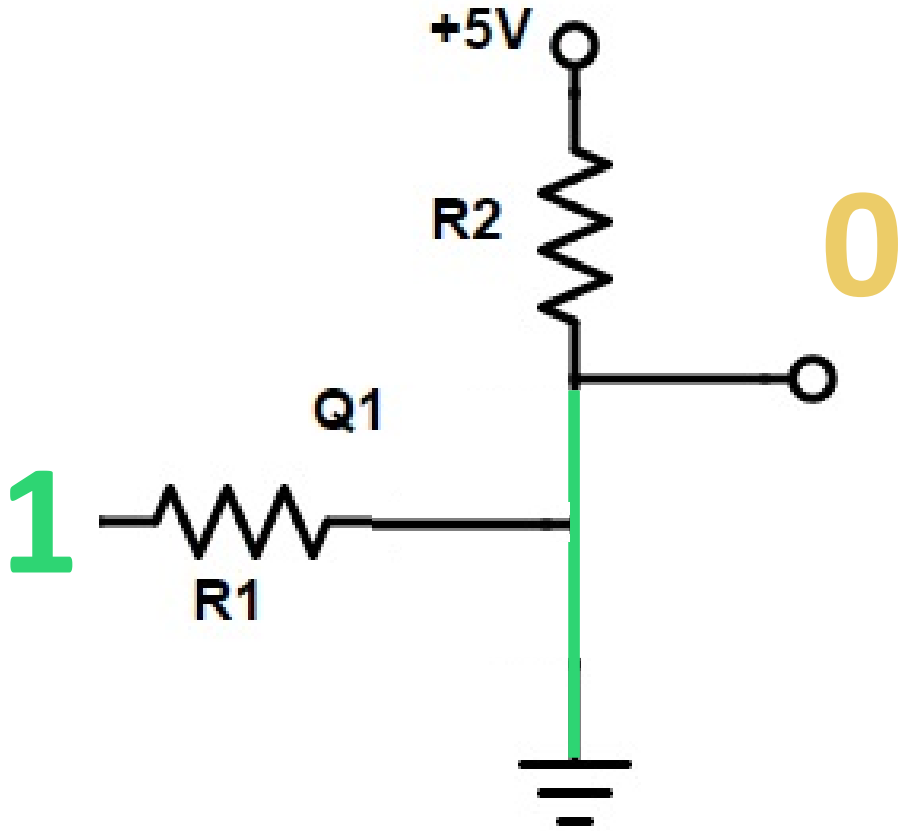


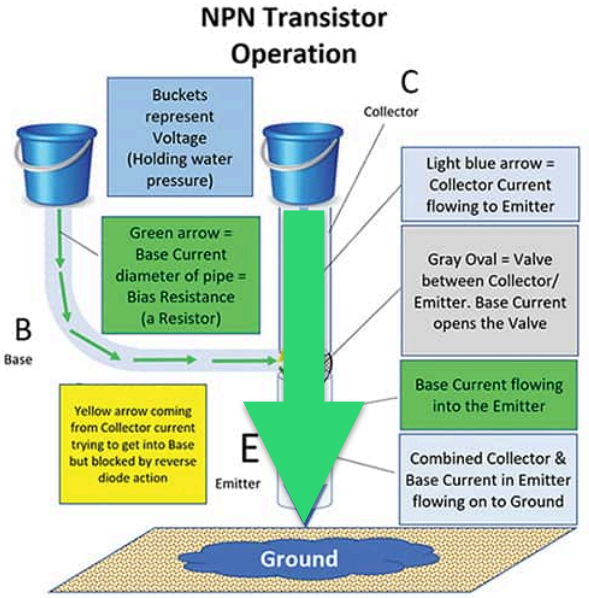
Puerta NOT con NPN



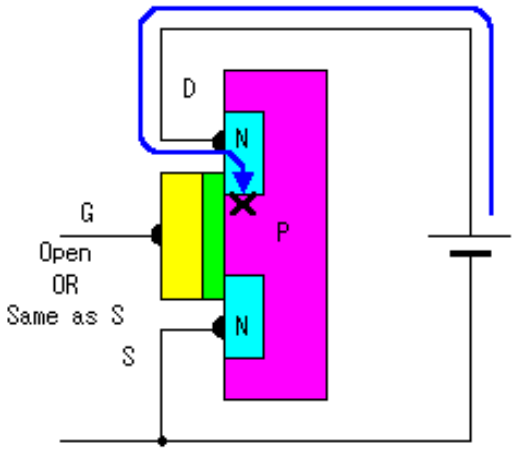


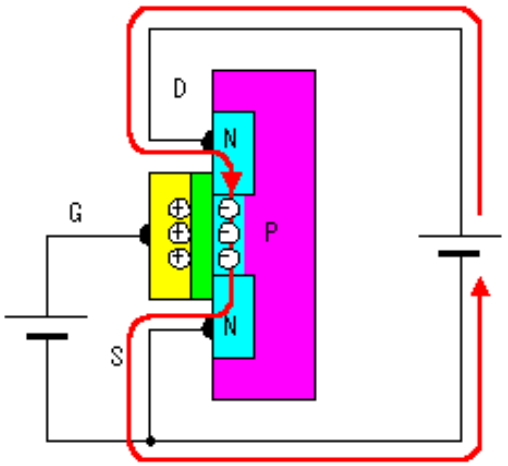
Puerta NOT con NPN



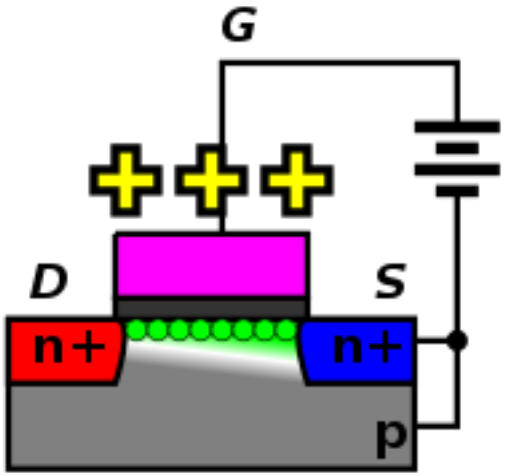


Transistor FET (Efecto de campo)

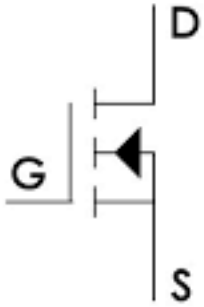




Gate
Source
Drain

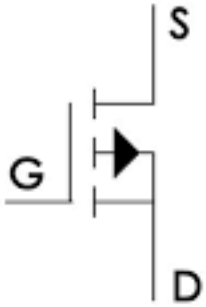


MOSFET Canal N



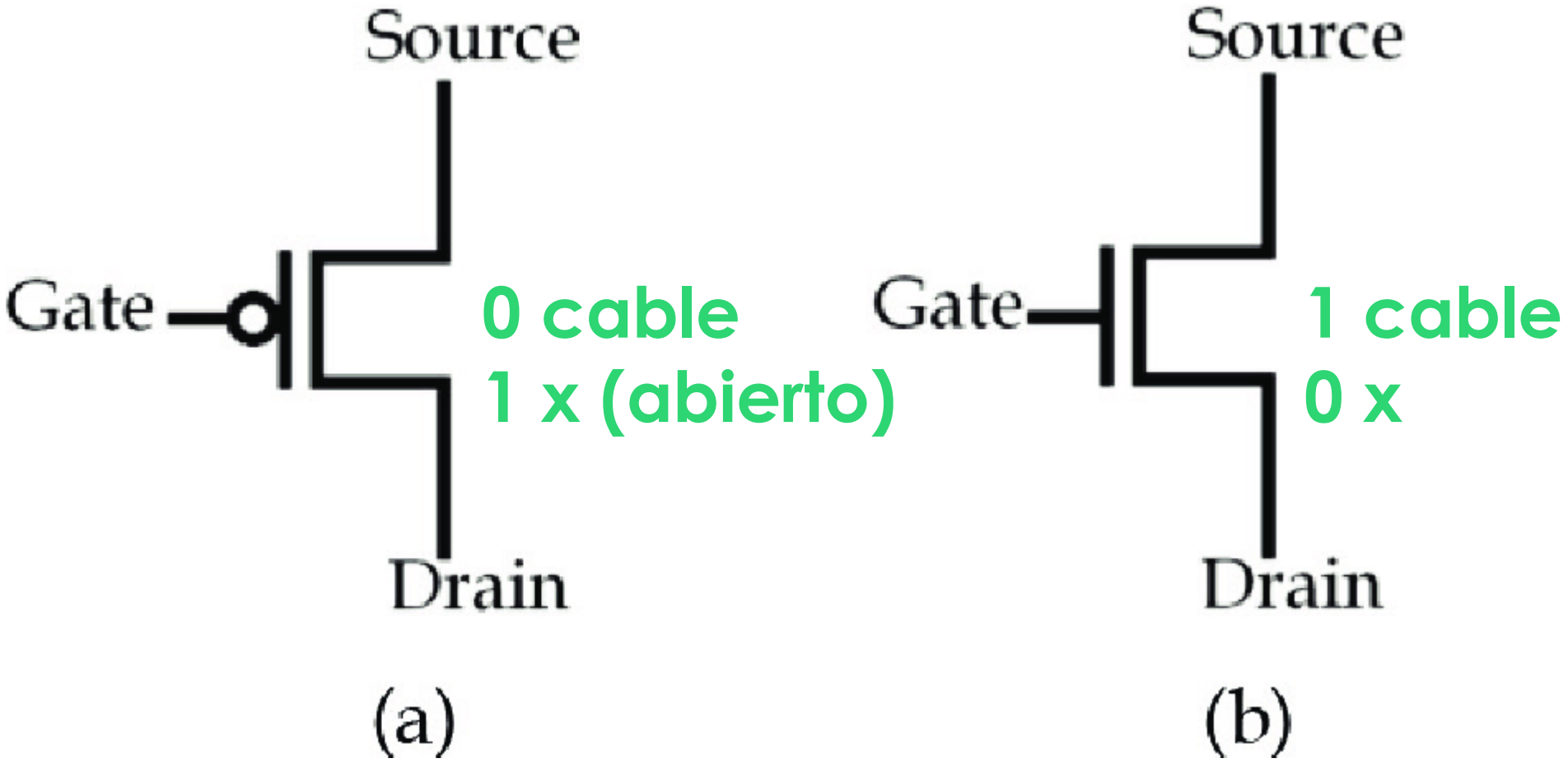
1 cable
0 x

MOSFET Canal P



0 cable
1 x

Transistor FET (Efecto de campo)



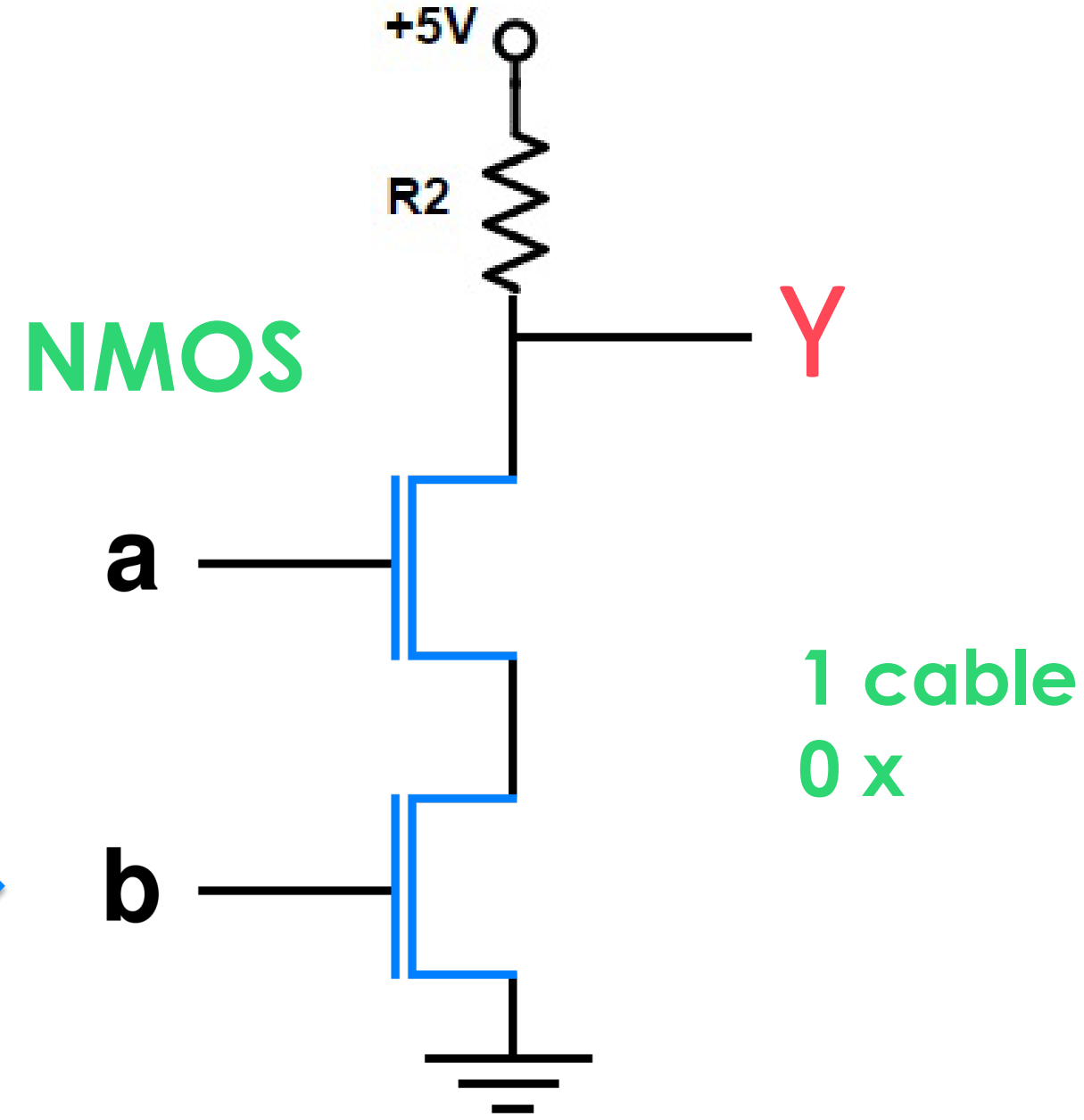
Con ellos se construyen puertas

$\overline{\text{CMOS}}$

Técnica constructiva en la que se utilizan **PMOS** y **NMOS** para construir puertas

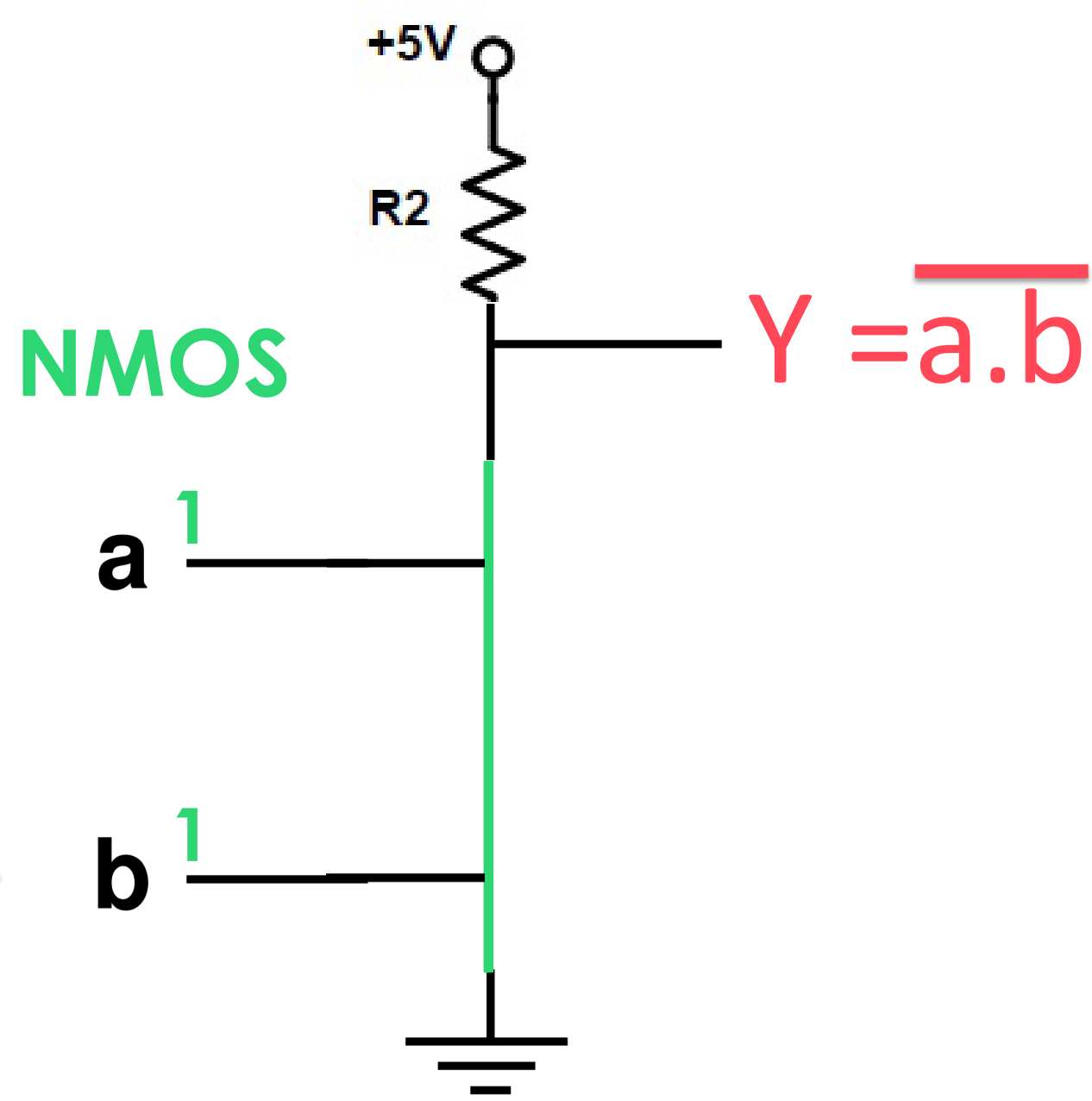
NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

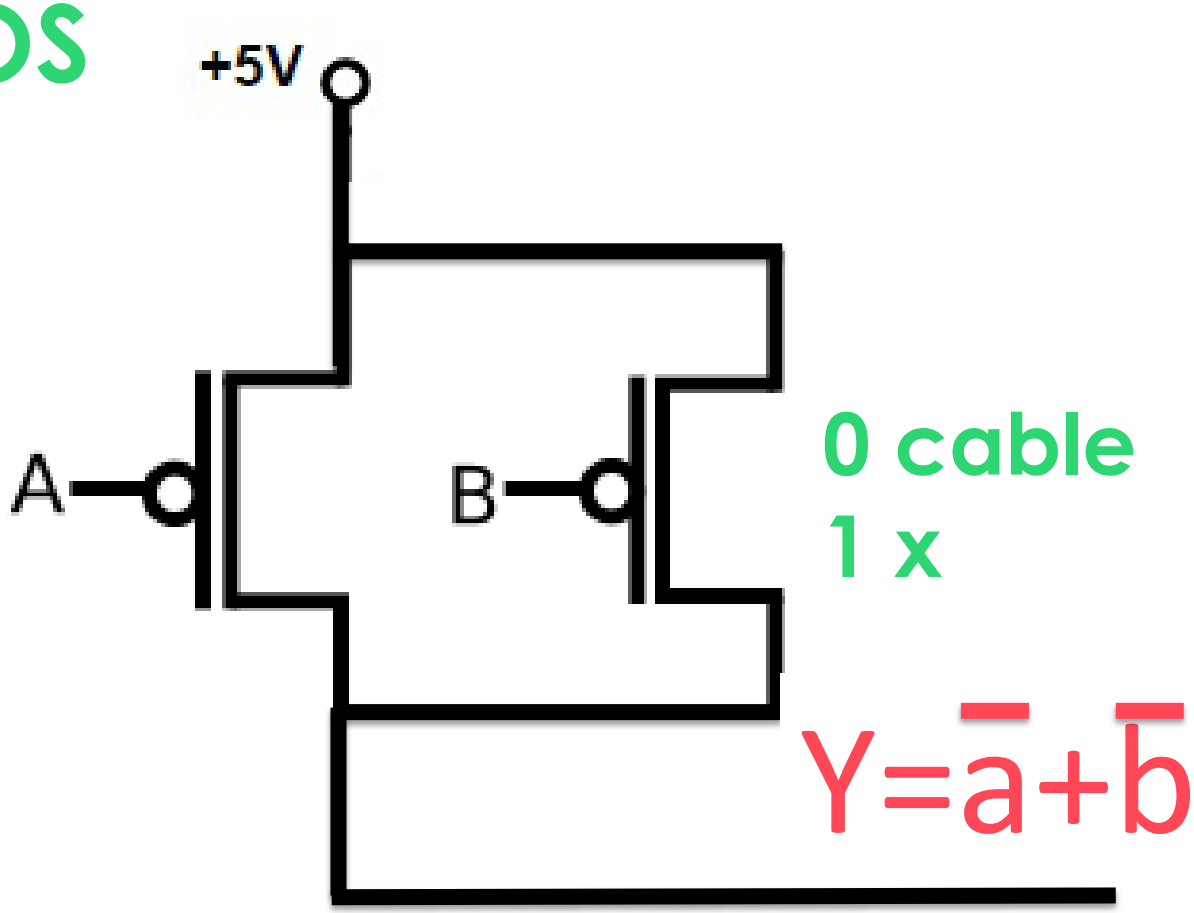


CMOS

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

PMOS



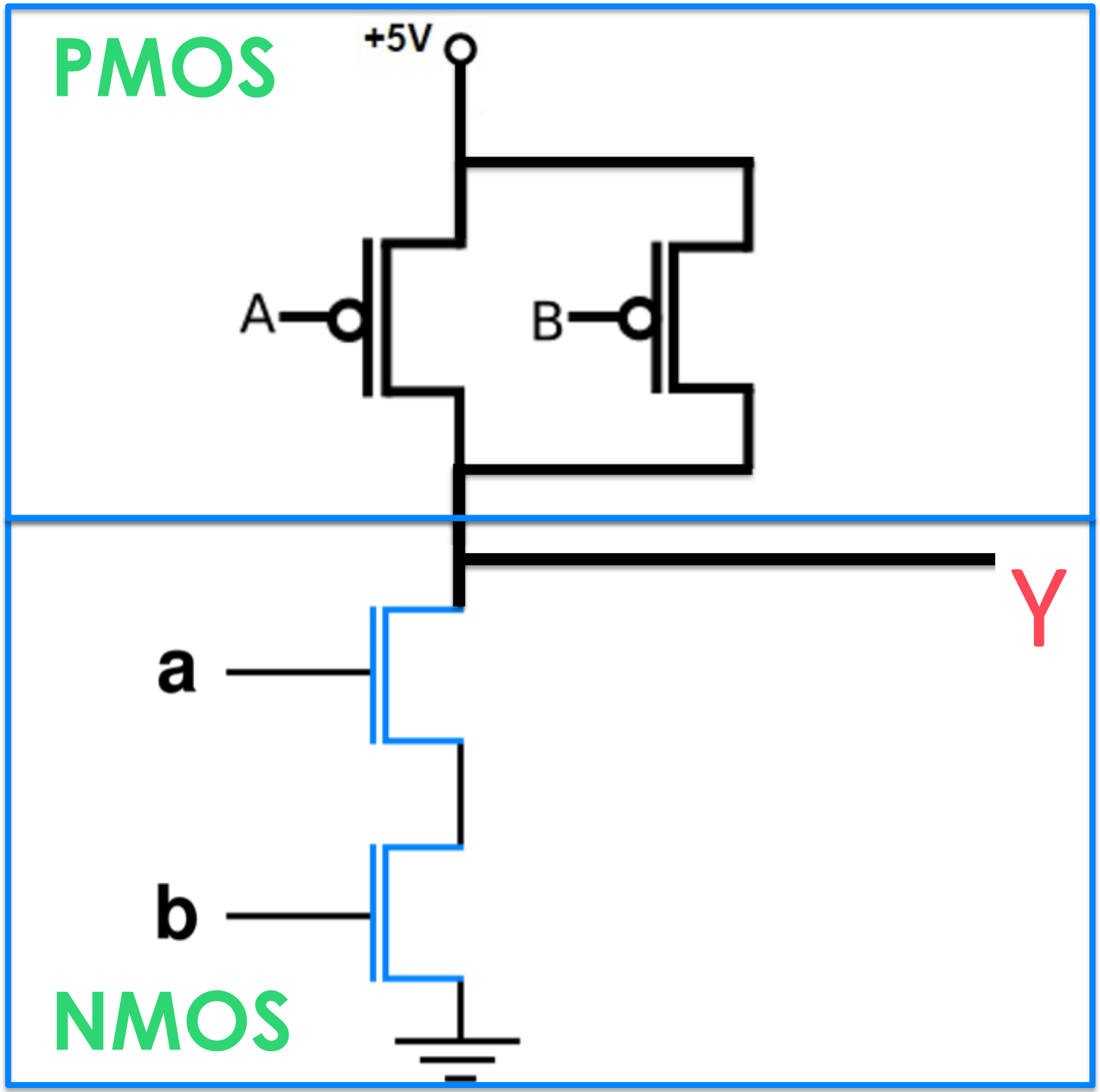
0 cable
1 x

$Y=\bar{a}+\bar{b}$

$Y=\bar{a}+\bar{b}=\overline{a.b}$

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



para construir **CUALQUIER** puerta:

un bloque para salida = 1

un bloque para salida = 0

solo 1 bloque se activa (NMOS o PMOS)

de todas las salidas a **1** se encarga **PMOS**

de todas las salidas a **0** se encarga **NMOS**

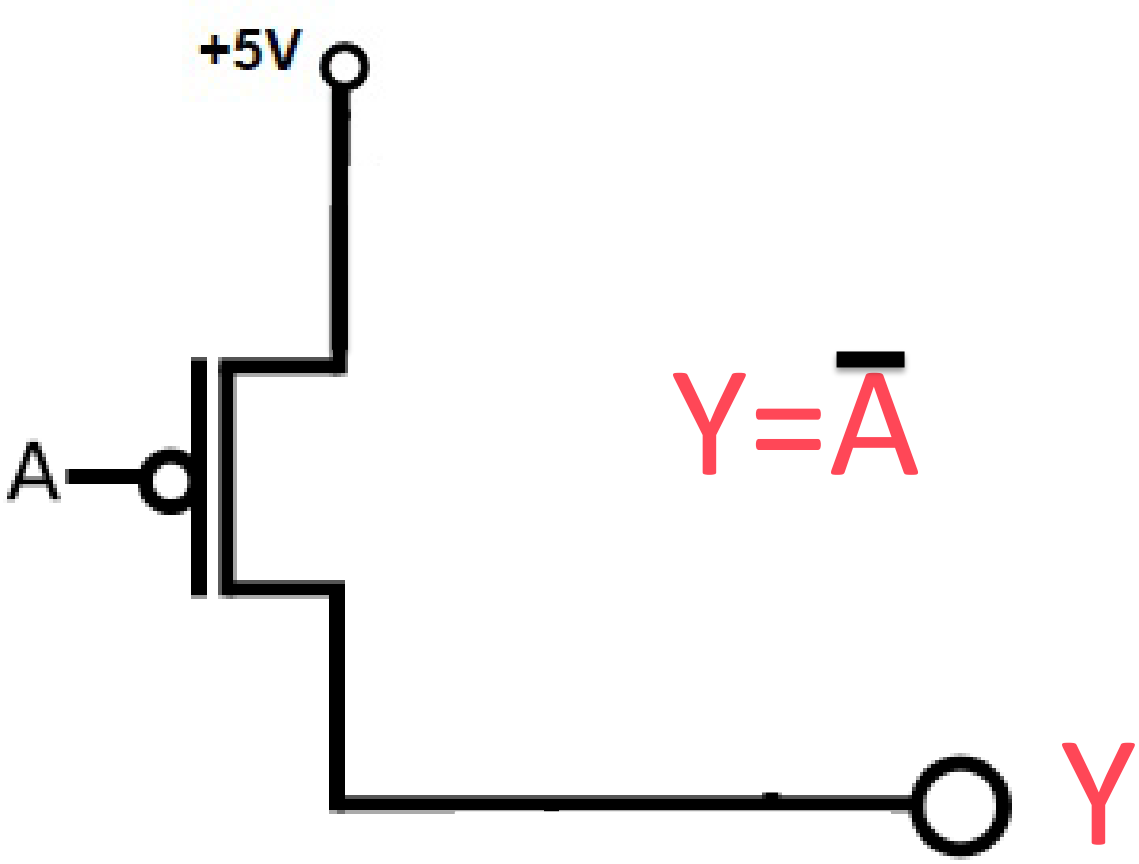

¿NOT ?
A Y
0 1
1 0

CMOS

PMOS

NOT

A	Y
0	1
1	0



CMOS

NOT

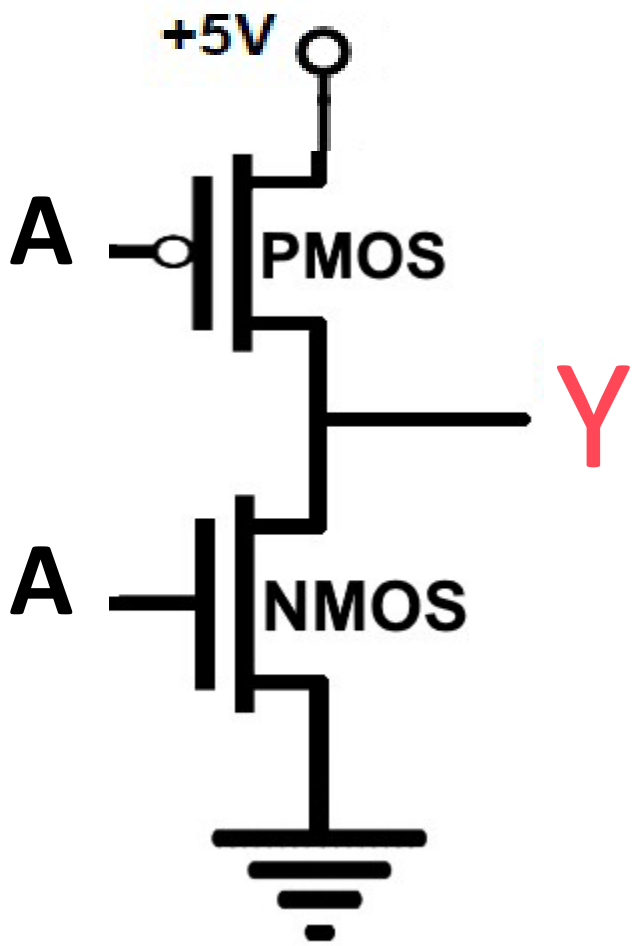
A	Y
0	1
1	0

$Y=\overline{A}$

Para salida 1

$Y=\overline{A}$

Para salida 0

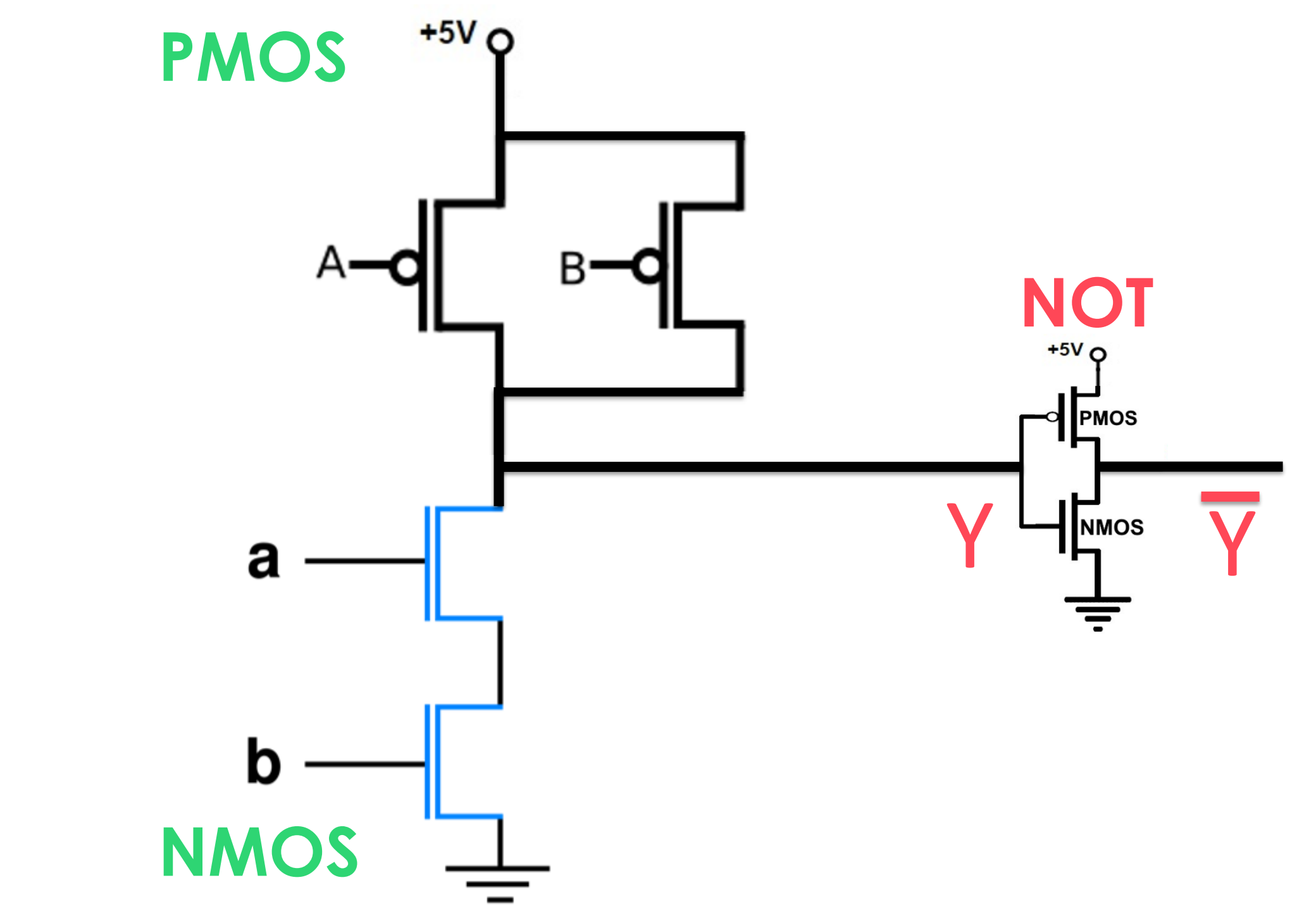


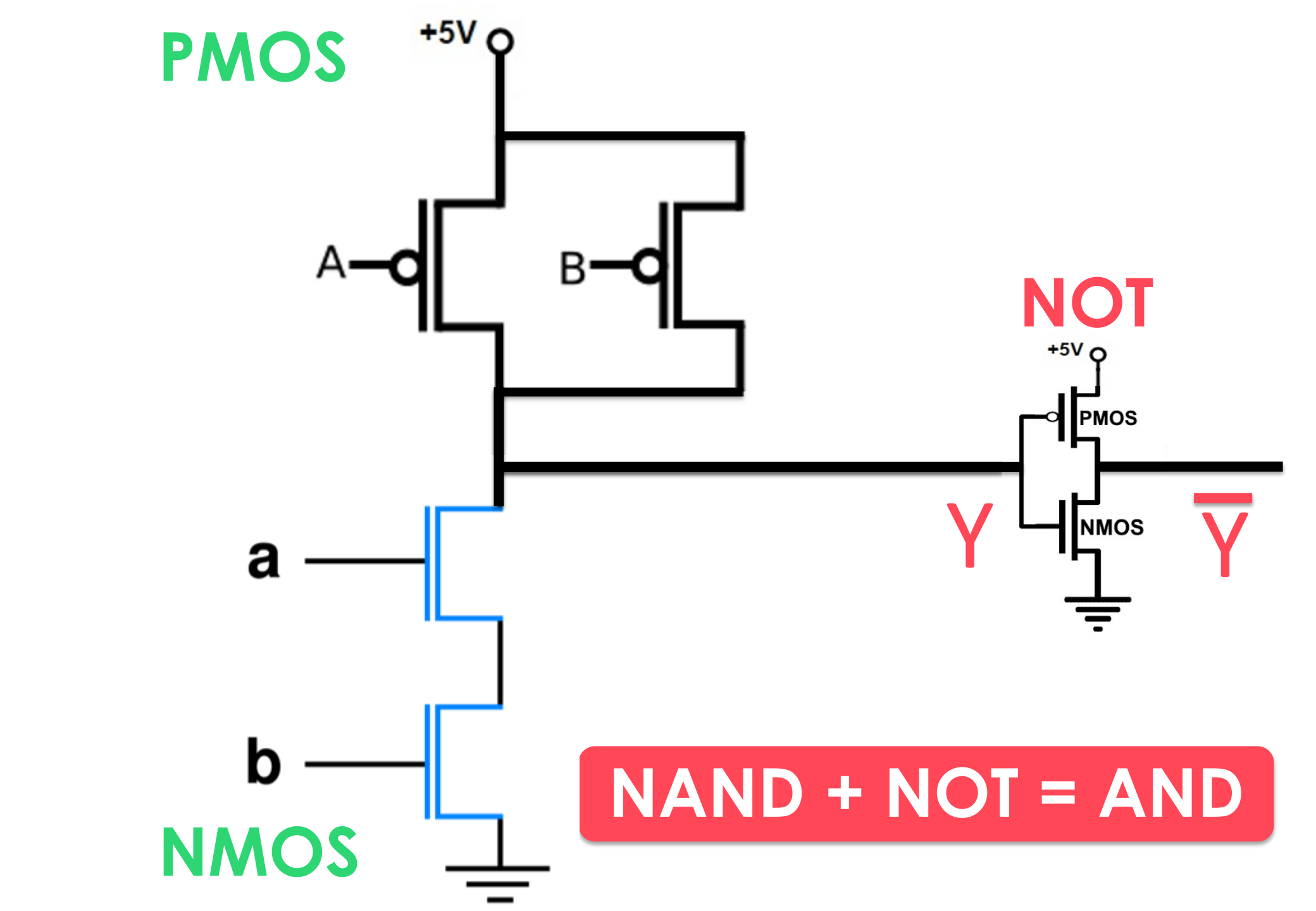
¿AND?

A	B	Salida
0	0	0
0	1	0
1	0	0
1	1	1

¿AND?

A	B	Salida
0	0	0
0	1	0
1	0	0
1	1	1


PMOS
+5V
A
B
NOT
+5V
PMOS
Y
NMOS
$\overline{Y}$
a
b
NMOS

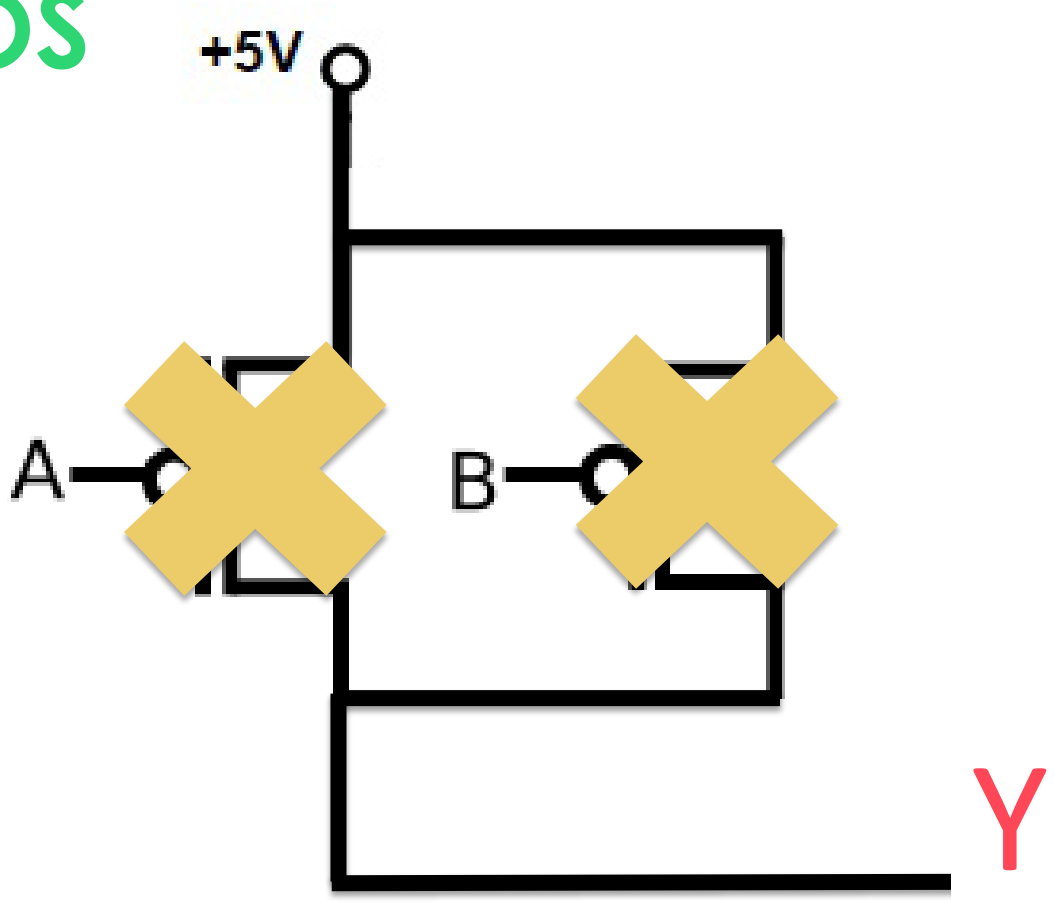

PMOS
+5V
A
B
NOT
+5V
PMOS
NMOS
Y
$\overline{Y}$
a
b
NMOS
NAND + NOT = AND


and...
¿directamente?

CMOS

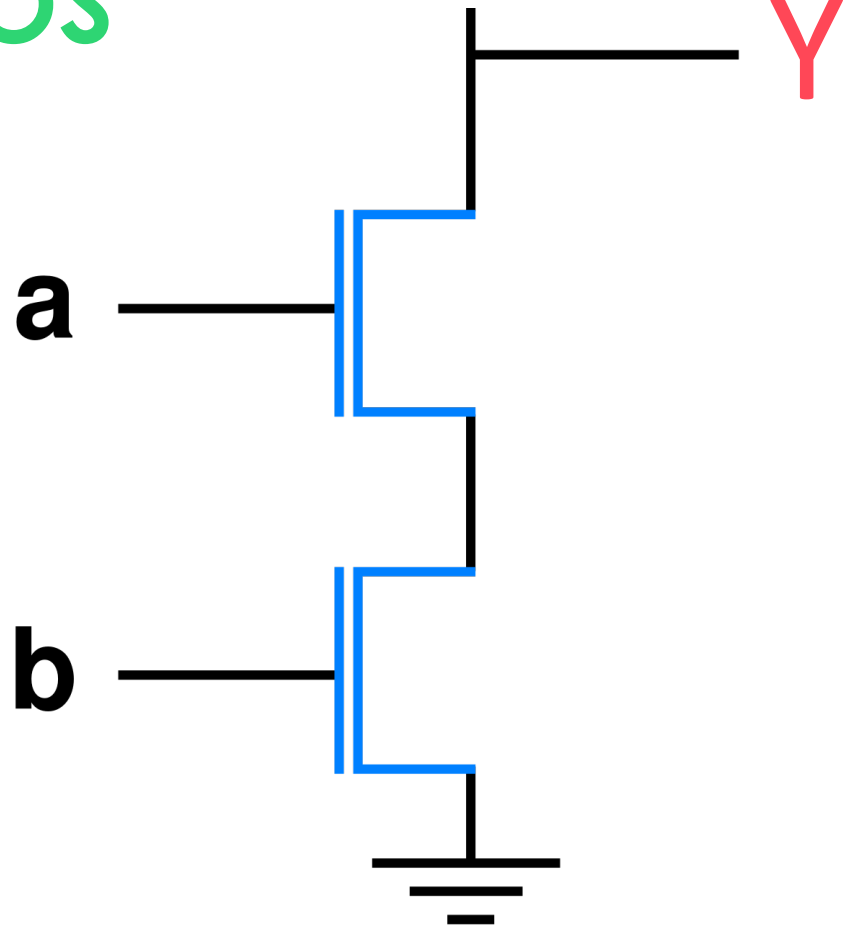
PMOS

A	B	Salida
0	0	0
0	1	0
1	0	0
1	1	1

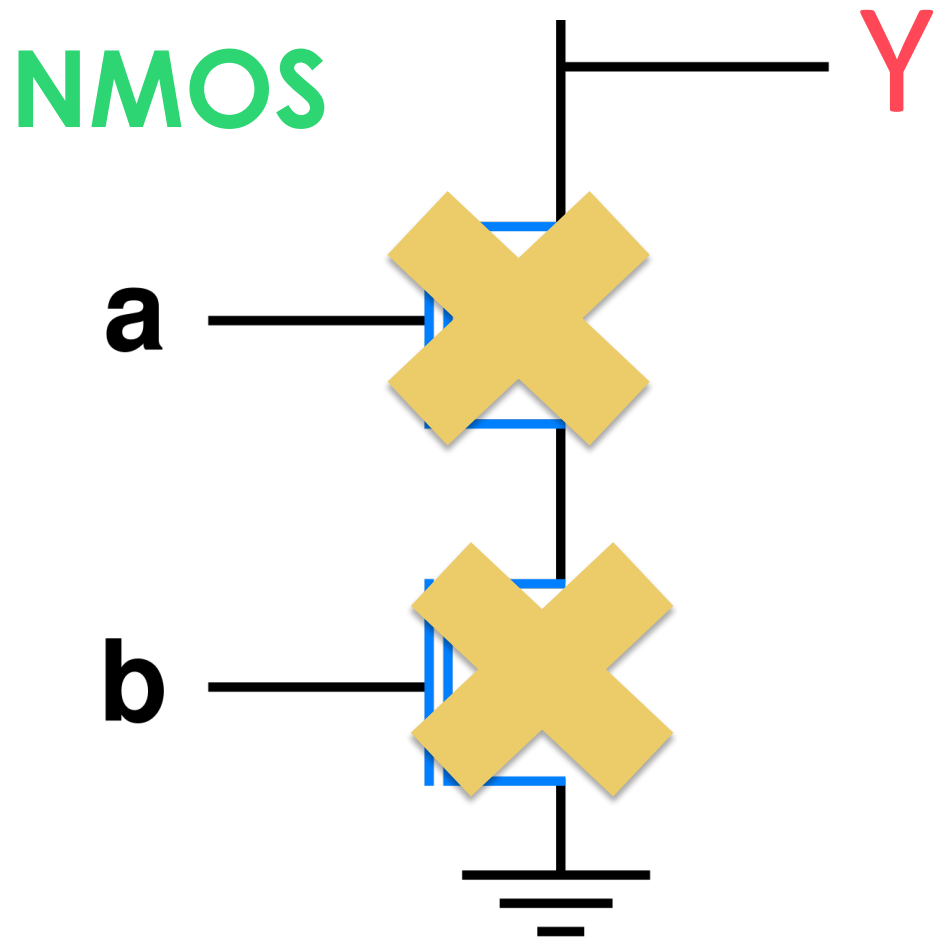


NMOS

A	B	Salida
0	0	0
0	1	0
1	0	0
1	1	1



A	B	Salida
0	0	0
0	1	0
1	0	0
1	1	1




NOR
A B Salida
0 0 1
0 1 0
1 0 0
1 1 0

NOR

A	B	Salida
0	0	1
0	1	0
1	0	0
1	1	0

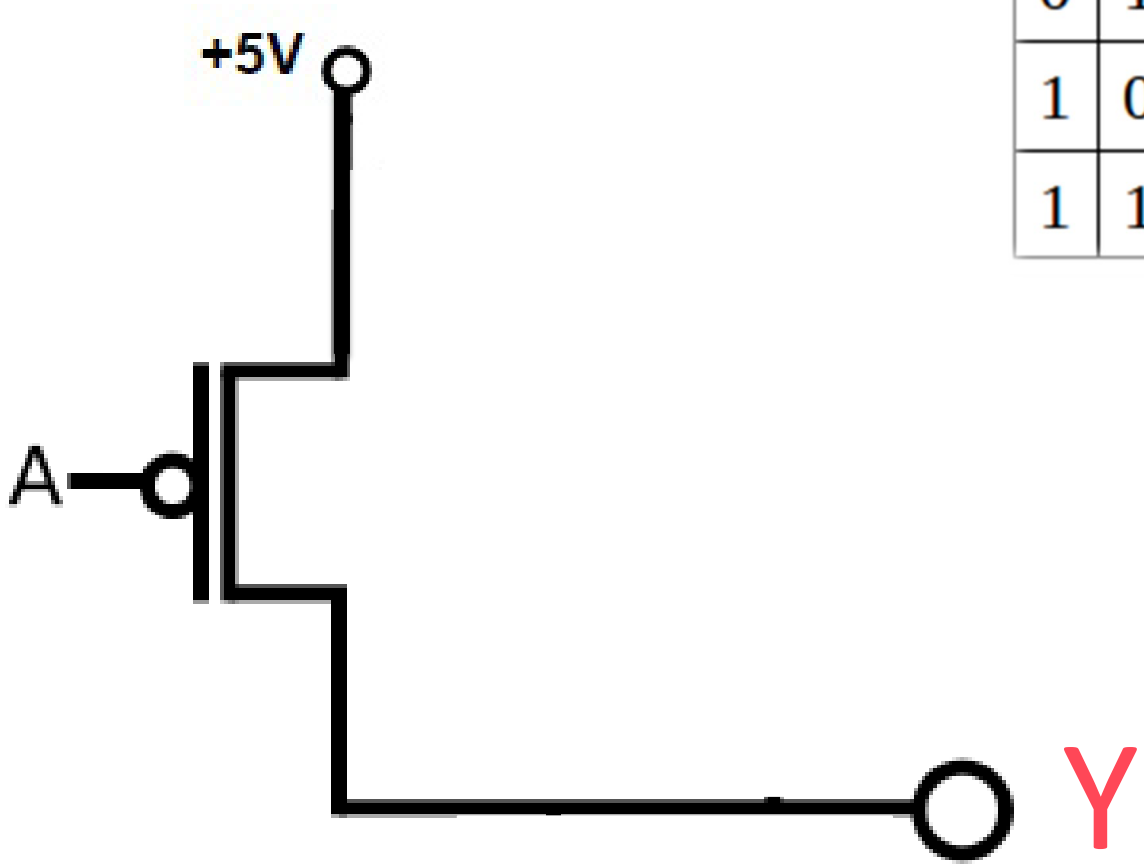
De todas las salidas a 1 se encarga PMOS

(para tener 1s, necesito 0s )

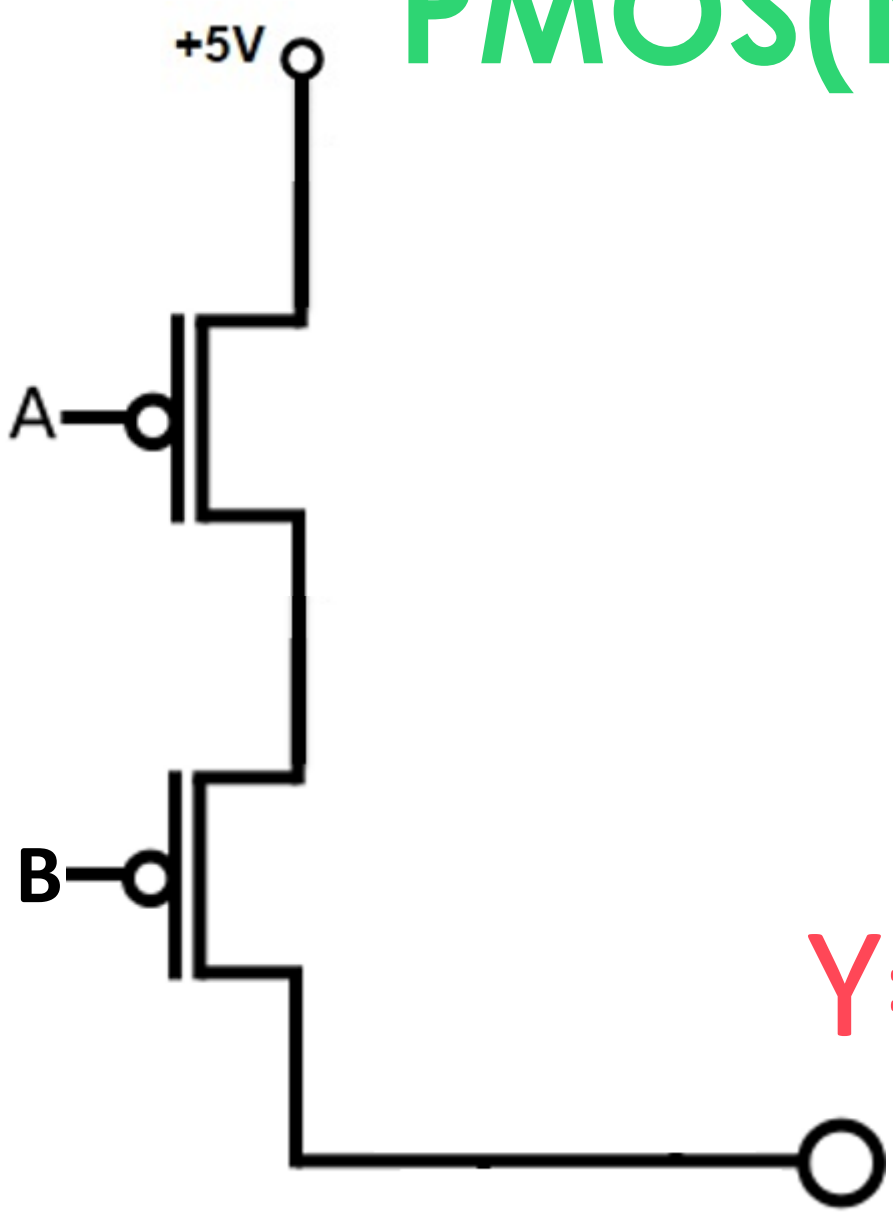
PMOS

A	B	Salida
0	0	1
0	1	0
1	0	0
1	1	0

0 cable
1 x (abierto)



PMOS(NOR)



A	B	Salida
0	0	1
0	1	0
1	0	0
1	1	0

$$Y=\overline{A}.\overline{B}=\overline{A+B}$$

NOR

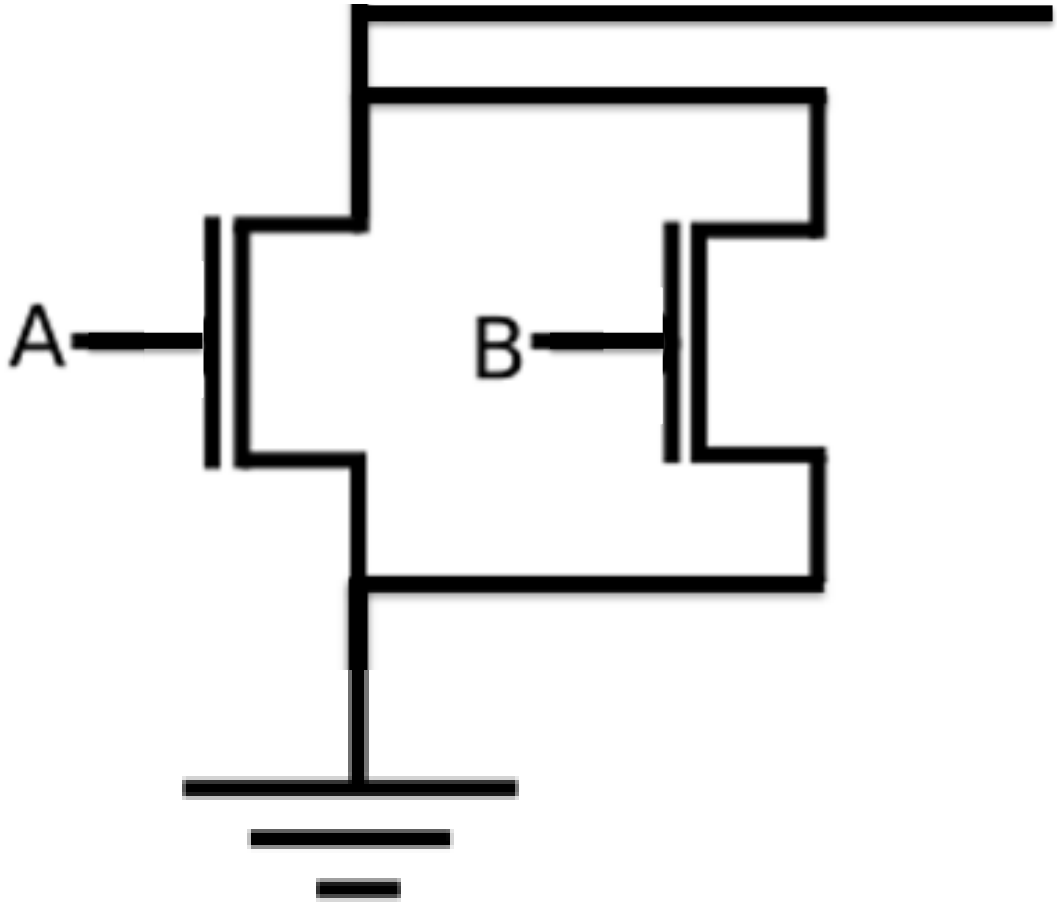
A	B	Salida
0	0	1
0	1	0
1	0	0
1	1	0

De todas las salidas a **0** se encarga **NMOS**

(para tener 0s, necesito 1s )

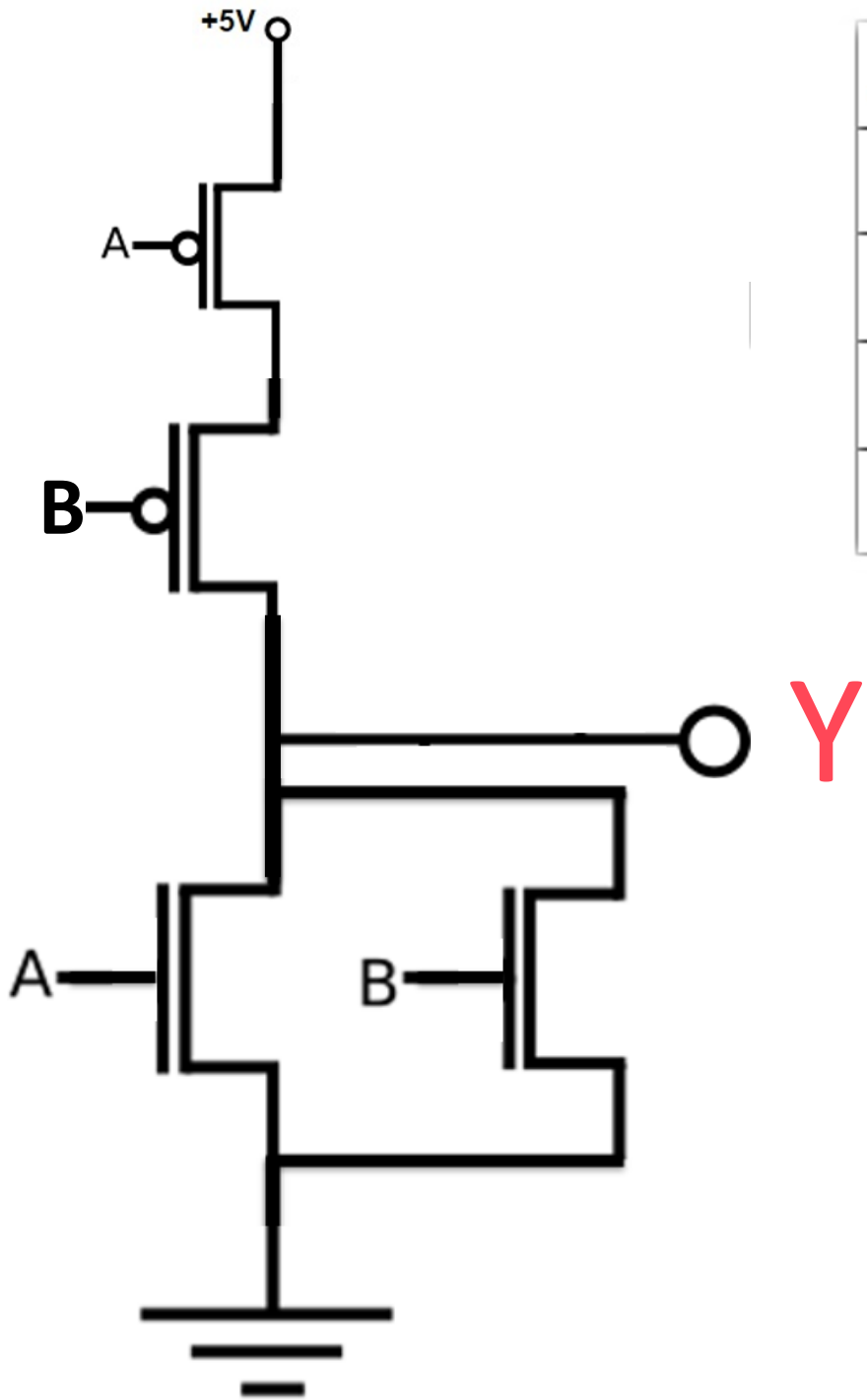
NMOS(NOR)

$$Y=\overline{A+B}$$



A	B	Salida
0	0	1
0	1	0
1	0	0
1	1	0

NOR



A	B	Salida
0	0	1
0	1	0
1	0	0
1	1	0