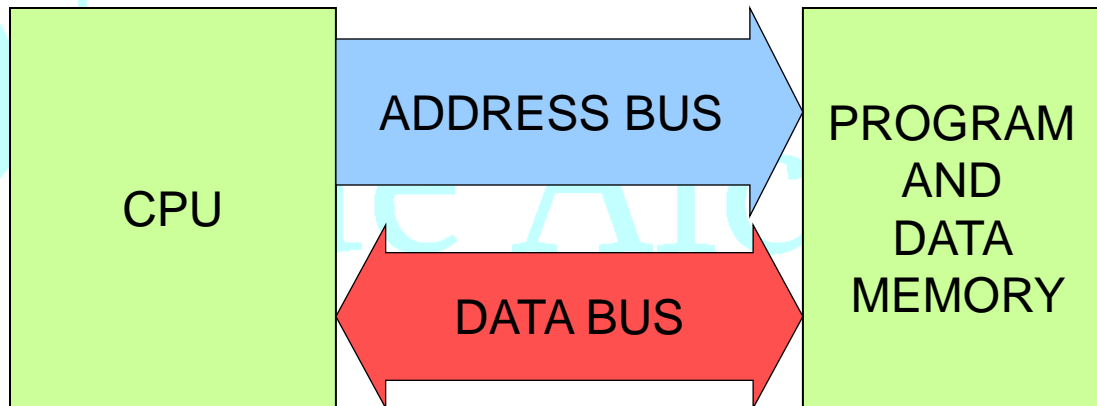# Topic 1

Pipelining

Department of Electronics

Academic Year 13/14

(ver 25-09-2013)

Evolution of microprocessors architecture
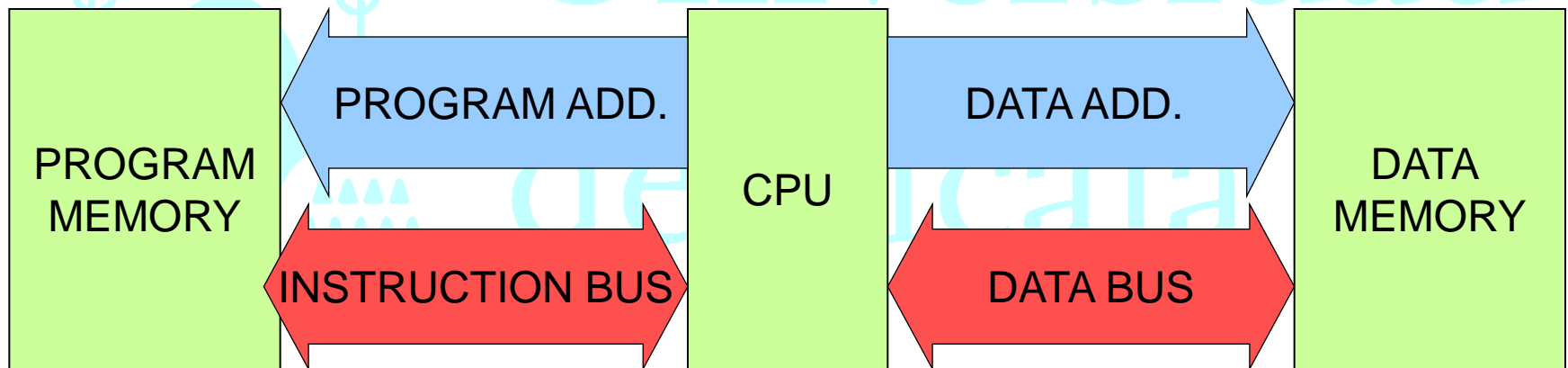
◆ Microprocessors Architectures: Von-Neuman

- ◆ Two busses: Address (**ADD**) and Data (**D**).

- ◆ Instructions and Data are accessed sequentially through the same Data Bus.

Evolution of microprocessors architecture

◆ **Microprocessors Architectures: Harvard**

- Two Address busses, a Data bus and an Instructions bus.

- Fetch the next instruction and move a data at the same time.

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Evolution of microprocessors architecture

◆ Pipelining

- ◆ Electronics design methodology for processors to overlap the execution of different instructions.

- ◆ At each pipe stage one part of the instruction is developed.

- ◆ A processor with N stages can run N instructions at the same time, increasing N times its efficiency.

- ◆ The efficiency increase is obtained just reorganizing instructions, no extra effort is needed in the CPU.

- ◆ On the other hand the design of the Control Unit is more complex, in order to get the best of the pipelining (do the best of instructions and their parts reorganization).
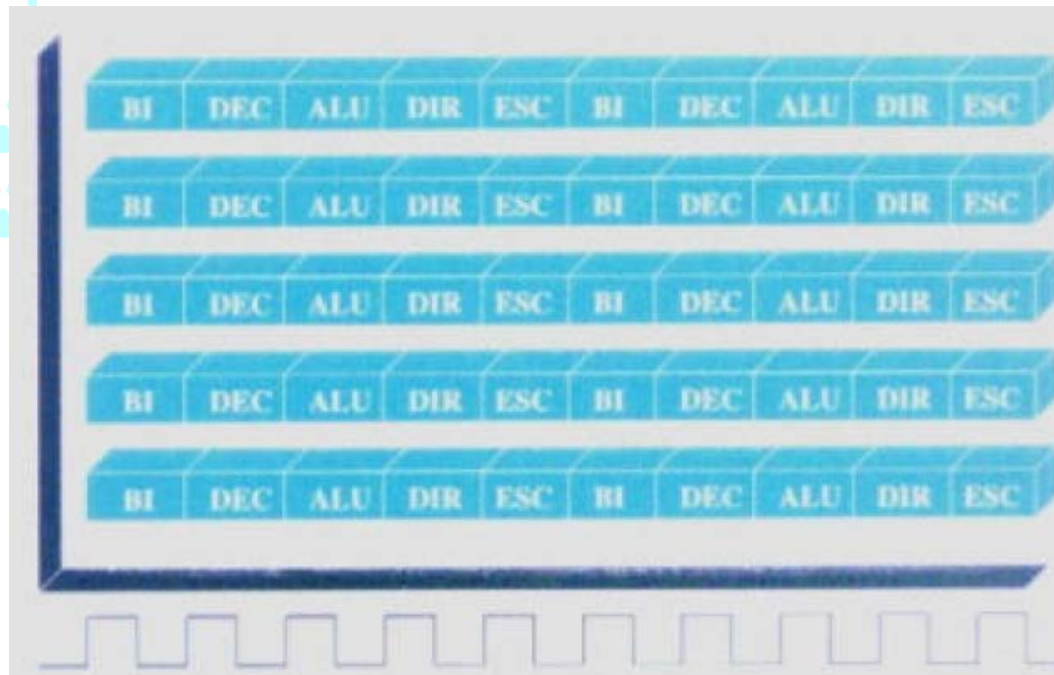
Evolution of microprocessors architecture

◆**Pipelining**

- ◆ The most used pipeline architecture in 90's had 5 stages: fetch (IF), decode (ID), operand read (MEM), execution (EX) and operand write back (WB).

- ◆ Nowadays normal pipelines have a bigger number of stages, for example 20 in Pentium IV.

2.8. Evolution of microprocessors architecture

◆**Super-scalar processors**

- Electronics design methodology to overlap the execution of different instructions using repeated functional units in the CPU.

- Processor with scalar level L has L repeated functional units that can thus run L instructions at the same time.

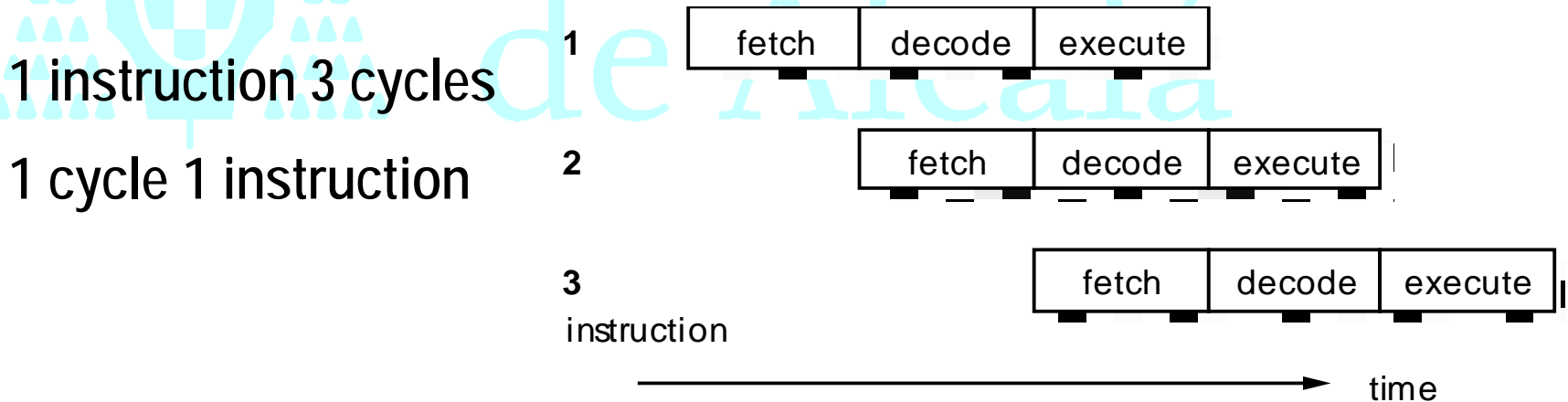# *Evolution of microprocessors architecture*

◆**Super-pipelining**

- Pipeline architecture in which slowest stages are divided in sub-stages in order to increase their speed.

- Two or more instructions can be execute different parts of the same stage at a moment.

- In a super-pipeline architecture the pipelining technology is applied twice: in a global context and internally in its functional units.

Evolution of microprocessors architecture

◆ **3 stages pipeline: Hazards and risks**

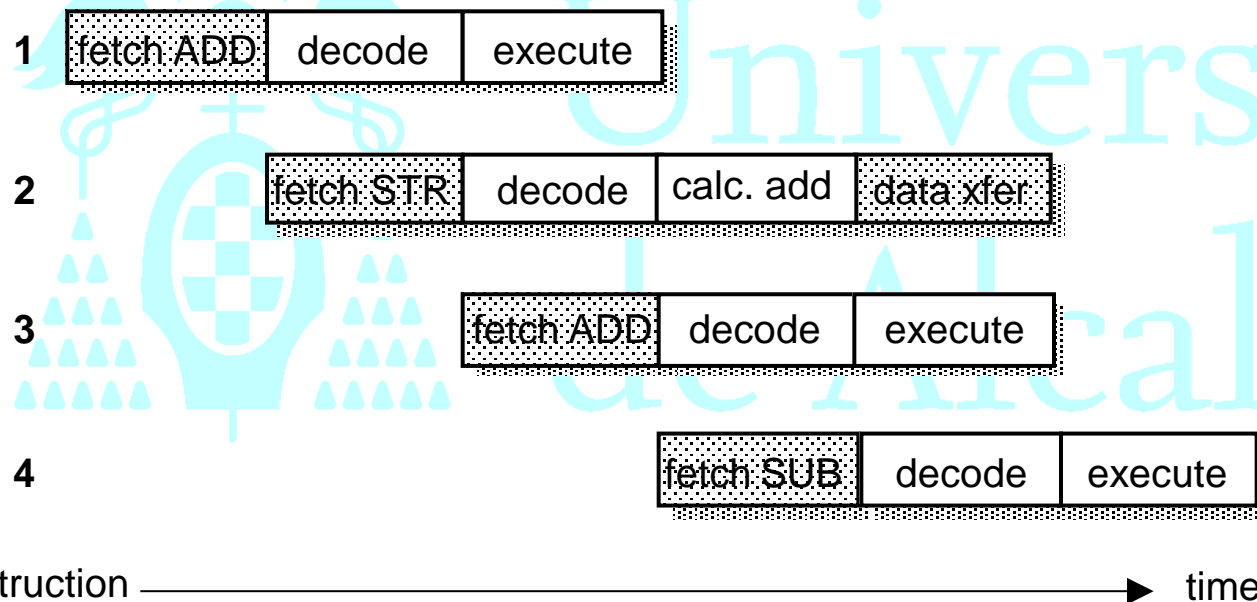- ◆ **Fetch:** The instruction is transferred from program memory and stored in the instructions pipeline

- ◆ **Decode:** The instruction is decoded

- ◆ **Execute:** ALU operations and data transferences

1 instruction 3 cycles

1 cycle 1 instruction

| 1 | fetch | decode | execute |

| 2 | fetch | decode | execute |

| 3 | fetch | decode | execute |

instruction

time

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Evolution of microprocessors architecture

◆ Multi-cycle instructions hazard

- ⬩ The instruction needs more cycles than the standard pipelined instructions

1	fetch ADD	decode	execute		

2		fetch STR	decode	calc. add	data xfer

3			fetch ADD	decode	execute

4				fetch SUB	decode	execute

instruction ⟶ time

Evolution of microprocessors architecture

◆ Structural hazard

   ♦ At a moment two instructions need the same hardware resources

1 | fetch ADD | decode | execute |

2 | fetch STR | decode | data xfer |

3 | fetch ADD | decode | execute |

4 | fetch ADD | decode | execute |

instruction ─────────────────────────► time

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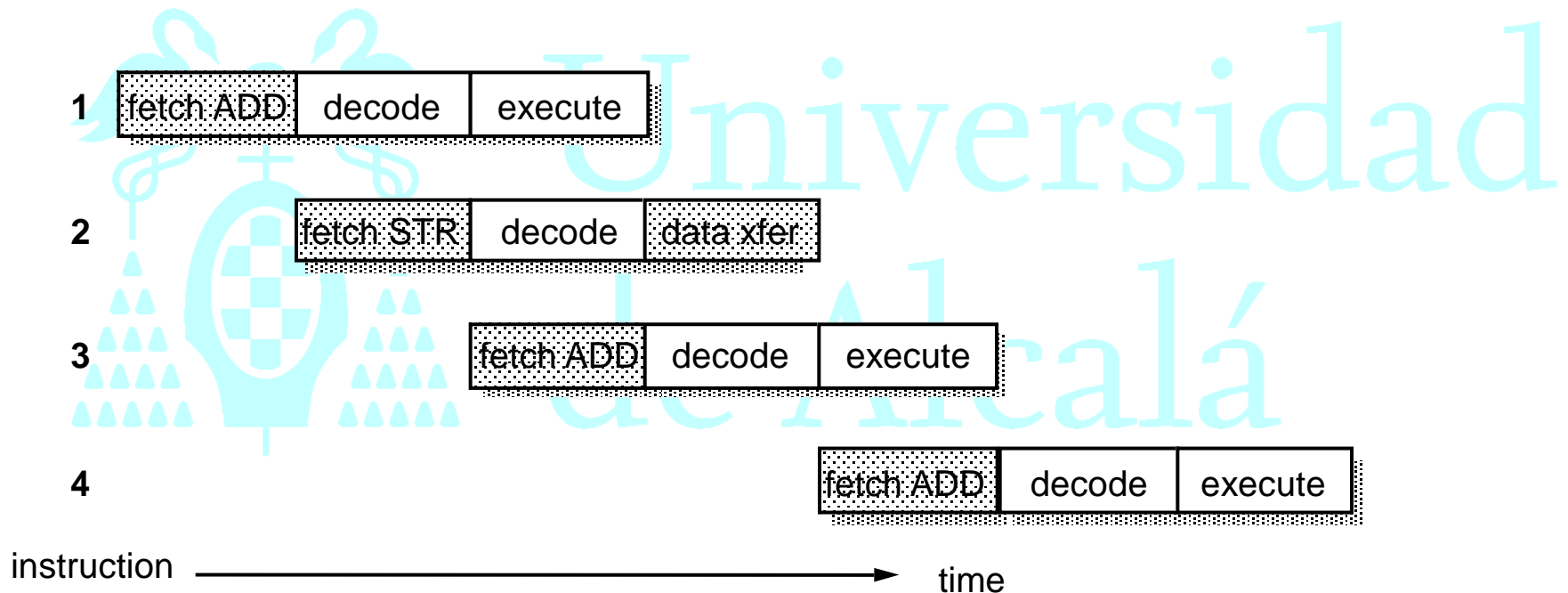
Evolution of microprocessors architecture

◆Control risk

• In conditional jumps, the pipeline may need to be emptied

1	fetch ADD	decode	execute
2	fetch BCC	decode	execute
3	fetch SUB	decode	
4	fetch STR		
5	fetch ADD	decode	execute

instruction ——————————————→ time

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