Lógica Secuencial en VHDL (III)

Timing

- Flip-flop samples D at clock edge

- D must be stable when sampled

- Similar to a photograph, D must be stable around clock edge
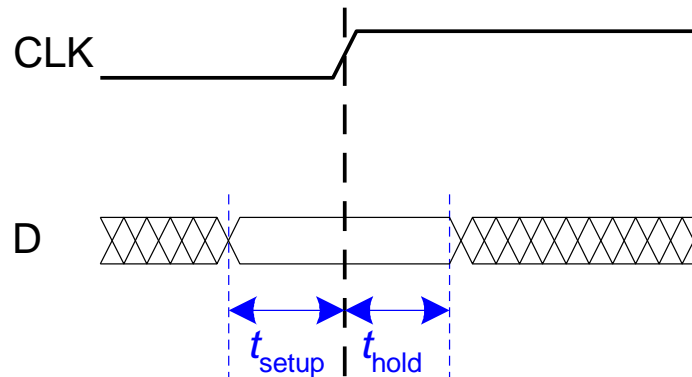
- If not, metastability can occur

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Input Timing Constraints

- **Setup time:** t_{setup} = time *before* clock edge data must be stable (i.e. not changing)
- **Hold time:** t_{hold} = time *after* clock edge data must be stable
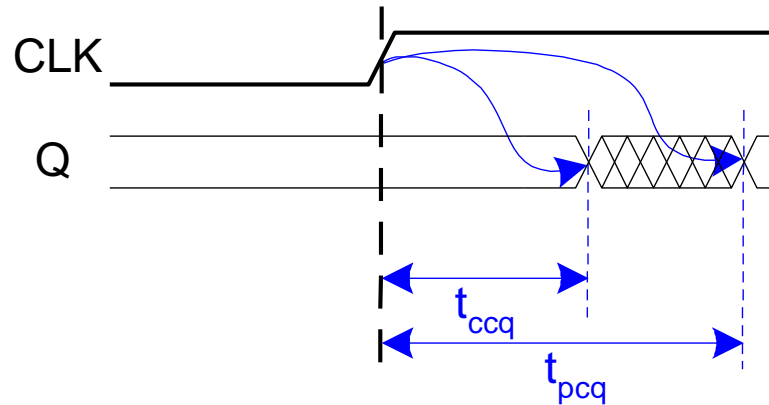- **Aperture time:** t_a = time *around* clock edge data must be stable ($t_a = t_{setup} + t_{hold}$)

CLK

D

t_{setup} t_{hold}

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Output Timing Constraints

- **Propagation delay:** t_{pcq} = time after clock edge that the output Q is guaranteed to be stable (i.e., to stop changing)
- **Contamination delay:** t_{ccq} = time after clock edge that Q might be unstable (i.e., start changing)

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Dynamic Discipline

- Synchronous sequential circuit inputs must be stable during aperture (setup and hold) time around clock edge

- Specifically, inputs must be stable
  - at least t_{setup} before the clock edge
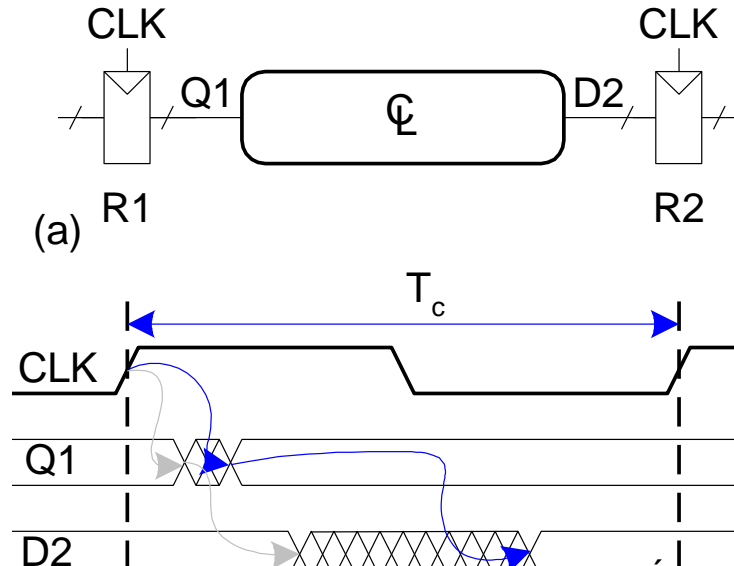 - at least until t_{hold} after the clock edge

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Dynamic Discipline

- The delay between registers has a **minimum** and **maximum** delay, dependent on the delays of the circuit elements

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Setup Time Constraint

- Depends on the **maximum** delay from register R1 through combinational logic to R2
- The input to register R2 must be stable at least t_{setup} before clock edge
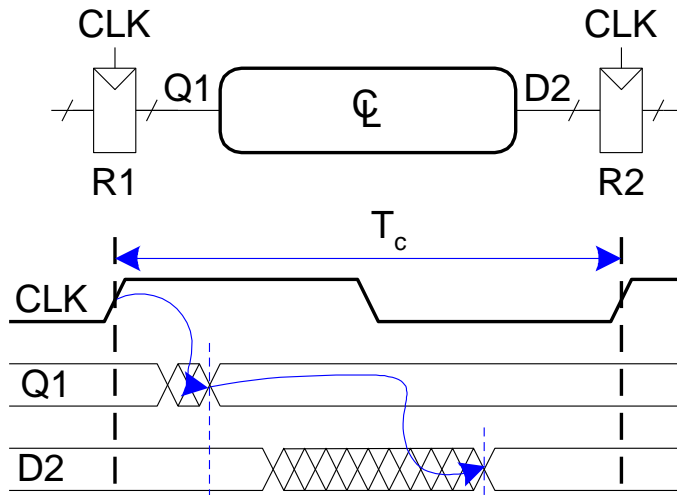
$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$
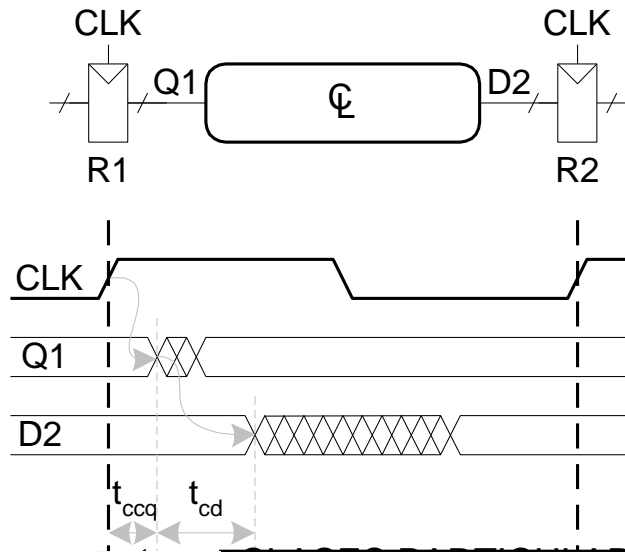
$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}})$$

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Hold Time Constraint

- Depends on the **minimum** delay from register R1 through the combinational logic to R2

- The input to register R2 must be stable for at least t_{hold} after the clock edge

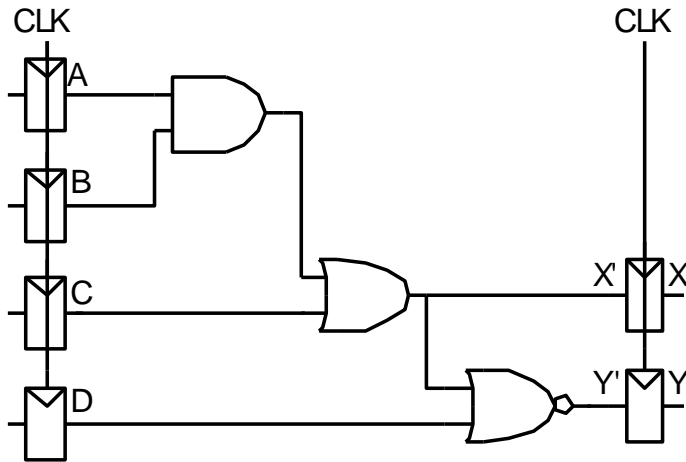$$t_{hold} < t_{ccq} + t_{cd}$$

$$t_{cd} > t_{hold} - t_{ccq}$$

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Timing Analysis

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{setup} = 60 \text{ ps}$$

$$t_{hold} = 70 \text{ ps}$$

per gate
$$\begin{cases} t_{pd} = 35 \text{ ps} \\ t_{cd} = 25 \text{ ps} \end{cases}$$

t_{pd} = 3 x 35 ps = 105 ps

t_{cd} = 25 ps

Setup time constraint:

$T_c \geq (50 + 105 + 60)$ ps = 215 ps

Hold time constraint:

$t_{ccq} + t_{cd} \geq t_{hold}$?

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Timing Analysis

Add buffers to the short paths:
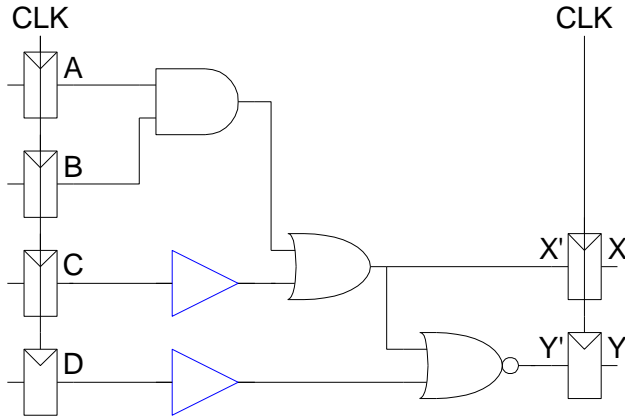
t_{pd} = 3 x 35 ps = 105 ps

t_{cd} = 2 x 25 ps = 50 ps

Setup time constraint:

$T_c \geq$ (50 + 105 + 60) ps = 215 ps

Timing Characteristics

t_{ccq} = 30 ps

t_{pcq} = 50 ps

t_{setup} = 60 ps

t_{hold} = 70 ps

t_{pd} = 35 ps

t_{cd} = 25 ps

per gate

Hold time constraint:

$t_{ccq} + t_{cd} > t_{hold}$?

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Clock Skew

- The clock doesn't arrive at all registers at same time
- **Skew:** difference between two clock edges
- Perform **worst case analysis** to guarantee dynamic discipline is not violated for any register – many registers in a system!

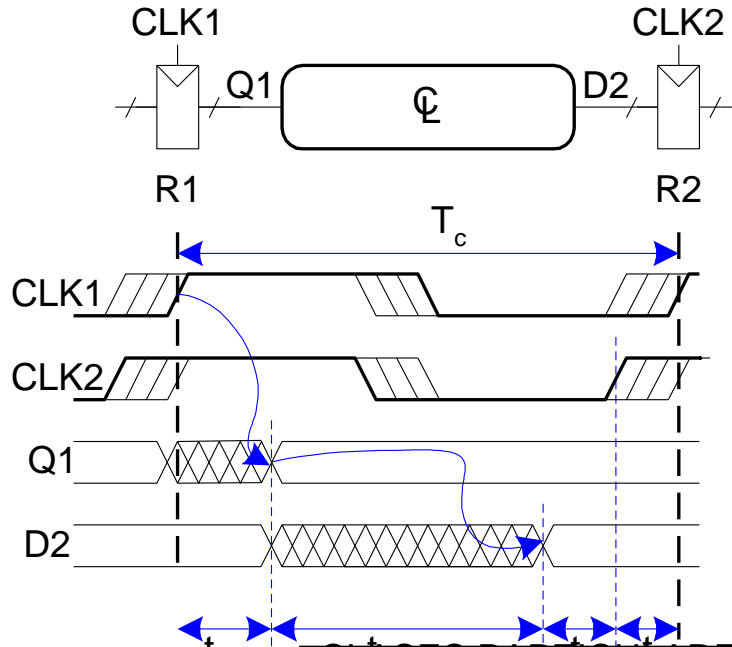# Setup Time Constraint with Skew

- In the worst case, CLK2 is earlier than CLK1

CLK1   CLK2

Q1   CL   D2

R1   R2

T_c

CLK1

CLK2

Q1

D2

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} + t_{\text{skew}}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}} + t_{\text{skew}})$$

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Hold Time Constraint with Skew

- In the worst case, CLK2 is later than CLK1
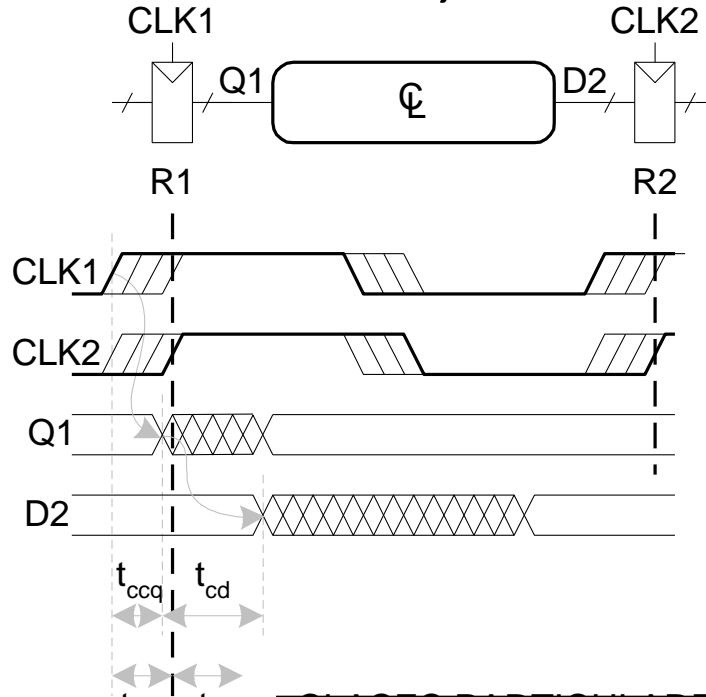
$$t_{ccq} + t_{cd} > t_{hold} + t_{skew}$$

$$t_{cd} > t_{hold} + t_{skew} - t_{ccq}$$

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