



COMPUTER

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- **MSI Protocol.**
- **MESI Protocol.**

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Request	State	Action type	Description
Read hit	S o M	Hit	Read data in local cache.
Read miss	I	Miss	Place read miss on bus.
Read miss	S	Replacement	Address conflict miss. Place read miss on bus.
Read miss	M	Replacement	Address conflict miss. Write back block, place read miss on bus
Write hit	M	Hit	Write data in local cache.
Write hit	S	Coherence	Place invalidate on bus.
Write miss	I	Miss	Place write miss on bus.
Write miss	S	Replacement	Address conflict miss. Place write miss on bus.
Write miss	M	Replacement	Address conflict miss. Write back block, place write miss on bus

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Request	State	Action type	Description
Read miss	S	-	Shared cache or memory service miss
Read miss	M	Coherence	Attempt to share data. Place cache block on bus and transition to shared.
Invalidate	S	Coherence	Attempt to write shared block. Invalidate block.
Write miss	S	Coherence	Attempt to write shared block. Invalidate block.
Write miss	M	Coherence	Attempt to write block that is exclusive elsewhere. Write-back cache block and make state invalid.

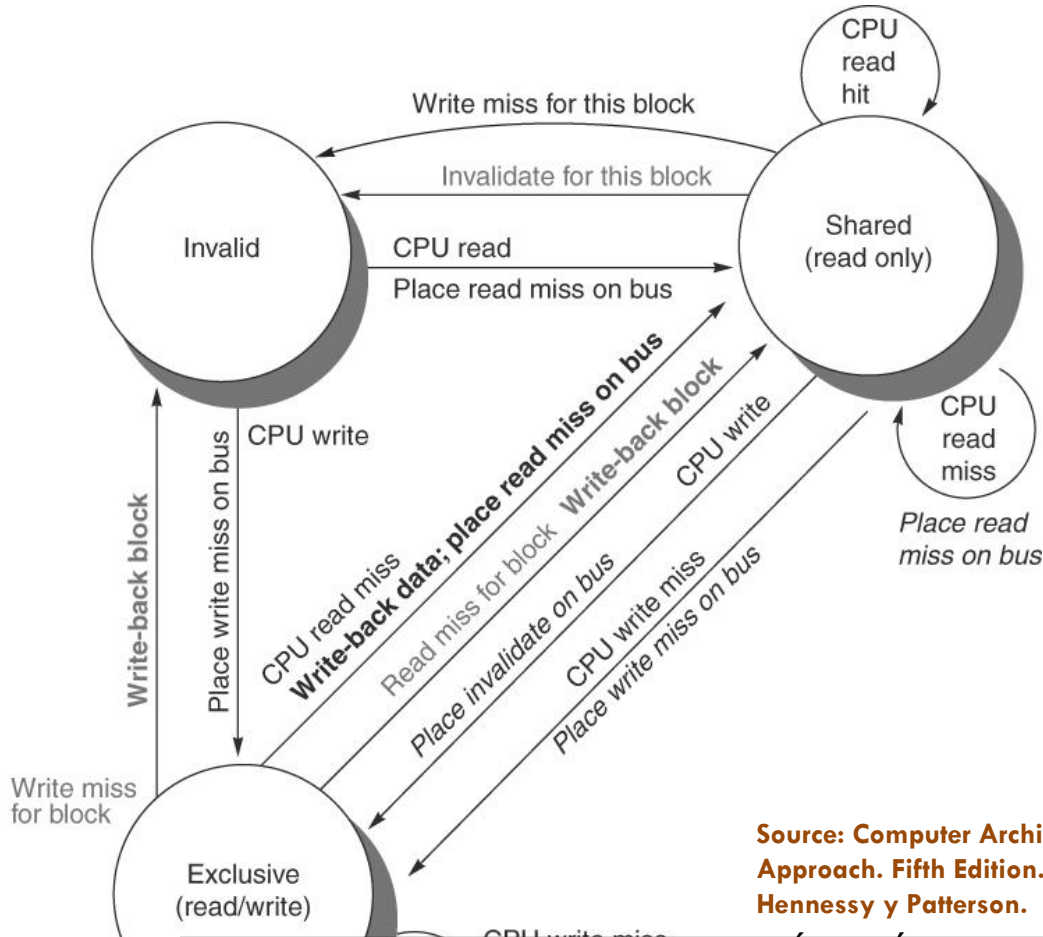


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Source: Computer Architecture. A Quantitative Approach. Fifth Edition. Hennessy y Patterson.

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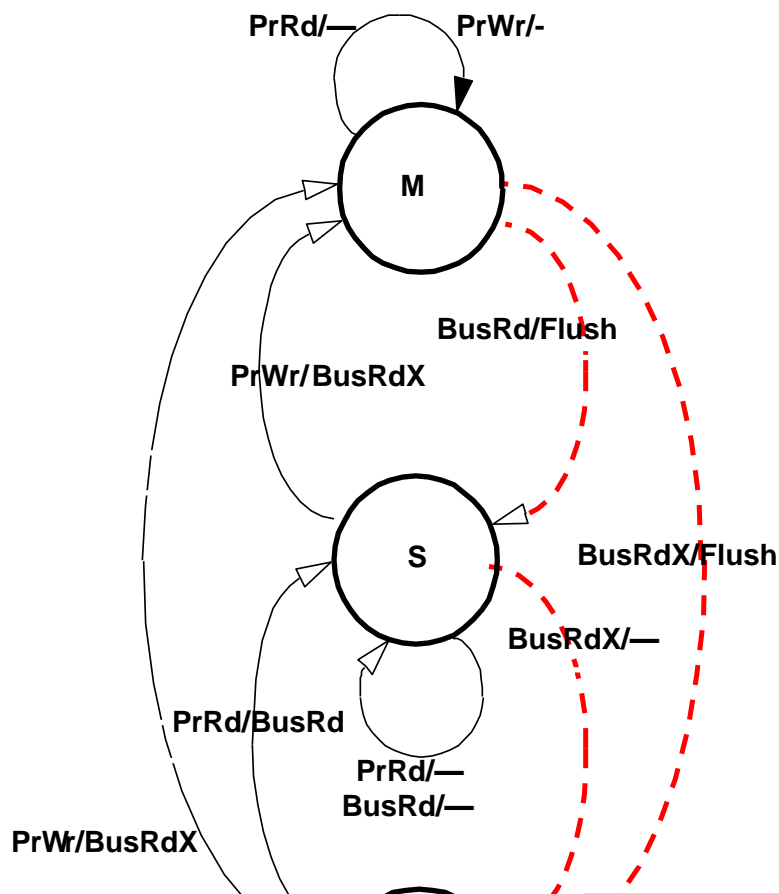
- **States:**
 - **Invalid (I):** Invalid block.
 - **Shared (S):** One or several copies of block.
 - **Dirty or Modified (M):** Only one copy.
- **Processor Events:**
 - **PrRd:** Processor Read.
 - **PrWr:** Processor Write.
- **Processor Transactions:**
 - **BusRd** (read): Request a copy of block without modifying.
 - **BusRdX** (read exclusive): Request a copy to modify.
 - **BusWB** (write back): Update memory.
- **Actions:**

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- Replacements and write backs not shown.
- No bus transactions due to:
 - ▣ Rd/Wr in M state.
 - ▣ Rd in S state.
- Two bus transactions for:
 - ▣ Rd/Wr in I state.
- Wr in S state causes two bus transactions:
 - ▣ Block transition to modified.
 - ▣ Transition can be avoided as data is already there:

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- Read and modify data are two bus transactions even if not shared.
 - ▣ Even in sequential programs!
 - ▣ BusRd (I- \rightarrow S) followed by BusRdX or BusUpgr (S- \rightarrow M)
- Solution:
 - ▣ Add new state: Exclusive (E).
- States:
 - ▣ M: Modified (dirty).
 - ▣ E: Exclusive (single non-modified copy).
 - ▣ S: Shared.

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- MSI Protocol.
- **MESI Protocol.**

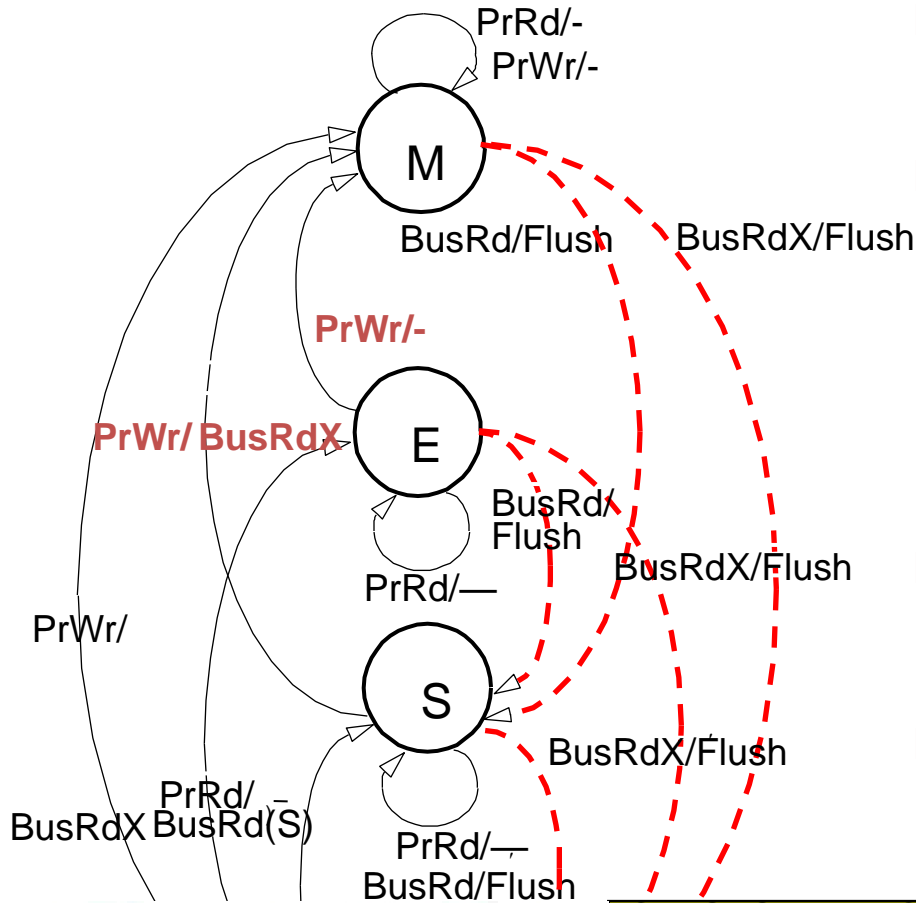
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- Hit: No transaction in bus in E state.
- Transitions from I:
 - ▣ To E with PrRd if no other processor has copy.
 - ▣ To S, otherwise.
- S, additional signal on bus.
- BusRd(S): If processor keeps block, set S signal to 1.

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